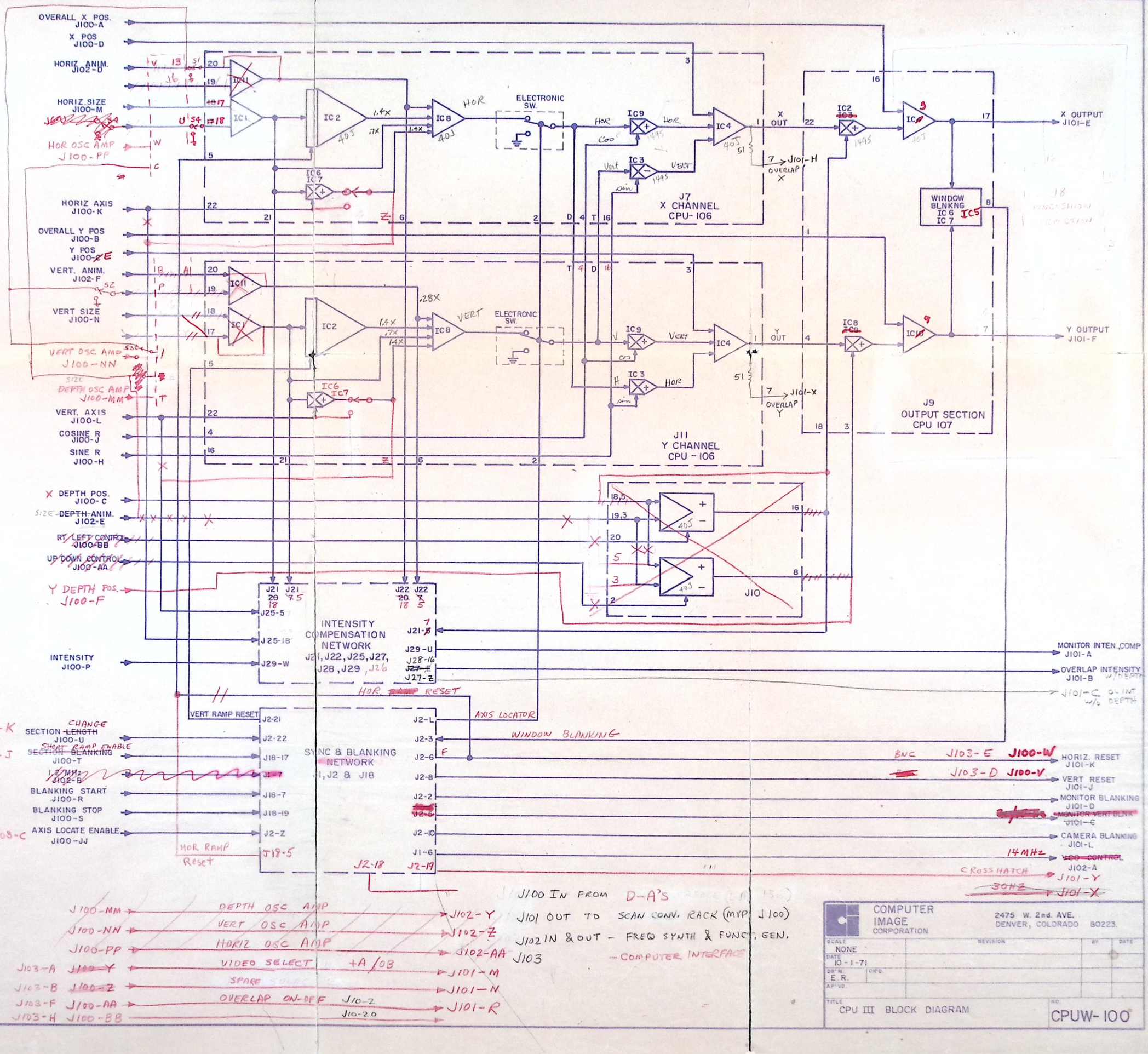
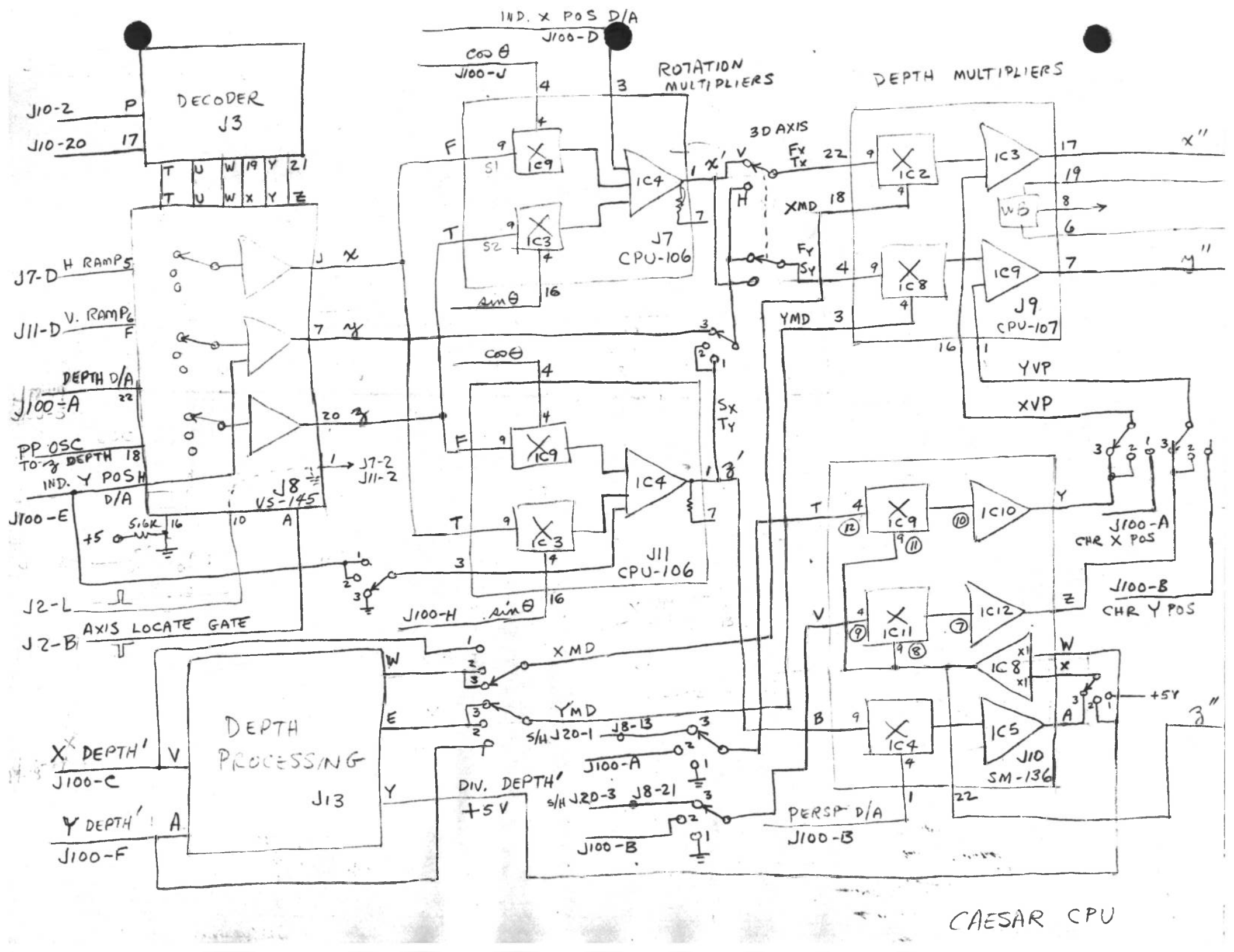
CORPORATION
CPU
CAESAR
~~PANCK~~
ALTEMUS

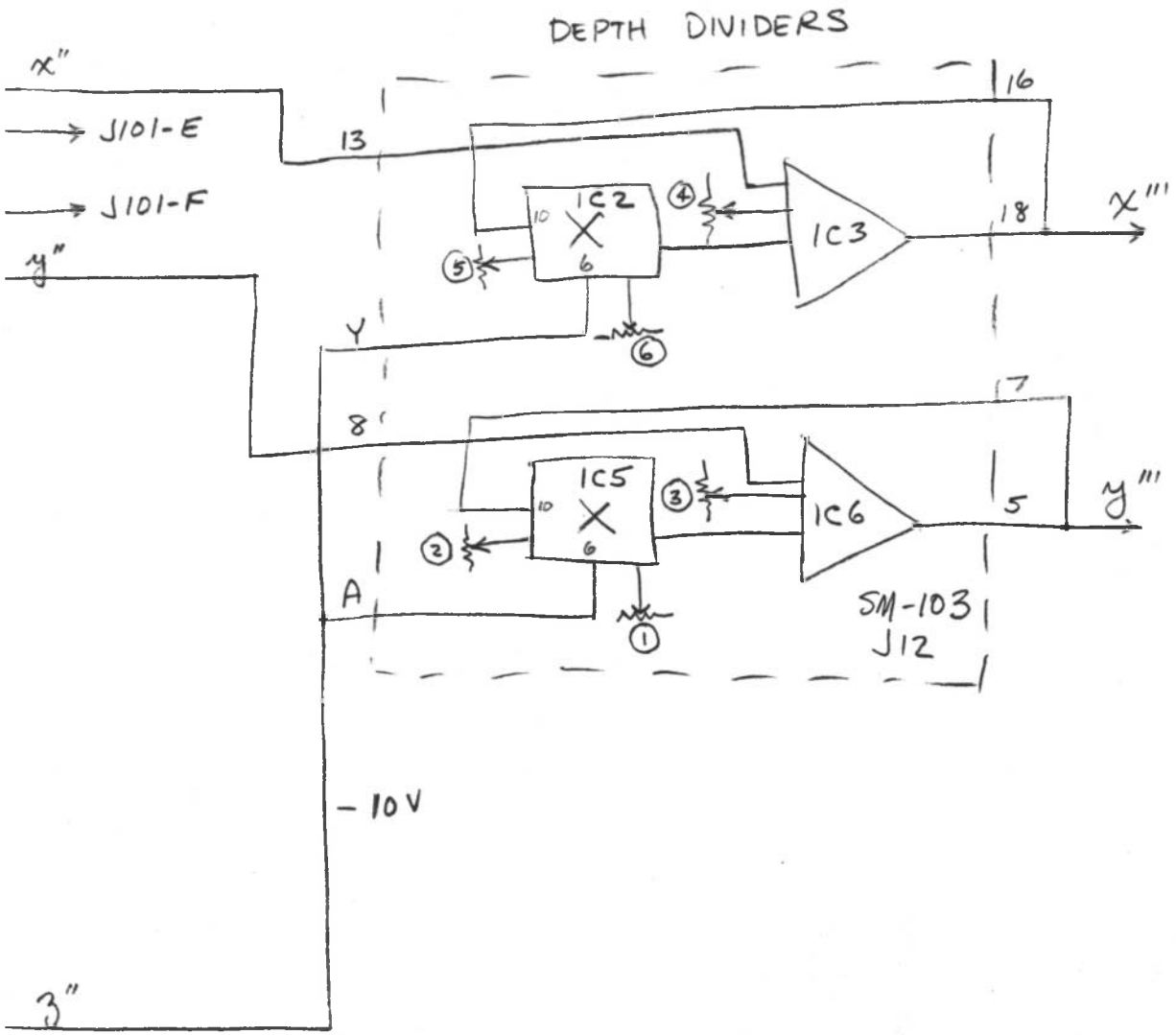
COMPUTER
IMAGE
CORPORATION

CPU
CAESAR

~~PANCK~~
ALTEMUS


OVERALL X POS. J100-A
X POS J100-D
HORIZ. ANIM. J102-D
HORIZ. SIZE J100-M
HOR OSC AMP J100-PP
HORIZ AXIS J100-K
OVERALL Y POS J100-B
Y POS J100-E
VERT. ANIM. J102-F
VERT SIZE J100-N
VERT OSC AMP J100-NN
SIZE DEPTH OSC AMP J100-MM
VERT. AXIS J100-L
COSINE R J100-J
SINE R J100-H
DEPTH POS. J100-C
SIZE-DEPTH-ANIM. J102-E
RT/LEFT CONTROL J100-BB
UP DOWN CONTROL J100-AA
Y DEPTH POS. J100-F
INTENSITY J100-P
IC11
IC1
IC2
IC8
ELECTRONIC SW.
IC9
IC3
IC4
IC6 IC7
X OUT
Y OUT
7 J101-H OVERLAP X
7 J101-X OVERLAP Y
J7 X CHANNEL CPU-106
J11 Y CHANNEL CPU-106
IC2
IC8
IC9
WINDOW BLNKNG IC6 IC7 IC5
J9 OUTPUT SECTION CPU 107
X OUTPUT J101-E
Y OUTPUT J101-F
J10
J21 J21
J22 J22
J25-5
J25-18
J29-W
J21-B
J29-U
J28-16
J27-Z
INTENSITY COMPENSATION NETWORK J21, J22, J25, J27, J28, J29, J26
HOR. RESET
VERT RAMP RESET
AXIS LOCATOR
WINDOW BLANKING
SYNC & BLANKING NETWORK J1, J2 & J18
J103-K CHANGE SECTION LENGTH J100-U
J103-J SHORT RAMP ENABLE SECTION BLANKING J100-T
14MHz J102-B
BLANKING START J100-R
BLANKING STOP J100-S
J103-C AXIS LOCATE ENABLE J100-JJ
HOR RAMP Reset
J18-5
J2-18
J2-19
MONITOR INTEN.,COMP J101-A
OVERLAP INTENSITY J101-B
J101-C
BNC J103-E J100-W HORIZ. RESET J101-K
J103-D J100-V VERT RESET J101-J
MONITOR BLANKING J101-D
CAMERA BLANKING J101-L
14MHz
CROSSHATCH J101-Y
30HZ J101-X
J100-MM DEPTH OSC AMP J102-Y
J100-NN VERT OSC AMP J102-Z
J100-PP HORIZ OSC AMP J102-AA
J103-A J100-Y VIDEO SELECT +A/B J101-M
J103-B J100-Z SPARE J101-N
J103-F J100-AA OVERLAP ON-OFF J10-2 J101-R
J103-H J100-BB J10-20
J100 IN FROM D-A'S
J101 OUT TO SCAN CONV. RACK (MYP J100)
J102 IN & OUT - FREQ SYNTH & FUNCT. GEN.
J103 - COMPUTER INTERFACE
COMPUTER IMAGE CORPORATION
2475 W. 2nd. AVE. DENVER, COLORADO 80223.
SCALE NONE
DATE 10-1-71
DR'N E.R.
CHK'D
APP'VD
REVISION
BY
DATE
TITLE CPU III BLOCK DIAGRAM
NO. CPUW-100


IND. X POS D/A
J100-D
DECODER
J3
J10-2
J10-20
ROTATION MULTIPLIERS
DEPTH MULTIPLIERS
3D AXIS
J7 CPU-106
J9 CPU-107
J11 CPU-106
J8 VS-145
J13
DEPTH PROCESSING
J10 SM-136
J7-D H RAMP
J11-D V. RAMP
DEPTH D/A
J100-A
PP OSC TO Z DEPTH
IND. Y POS D/A
J100-E
+5
5.6K
J7-2
J11-2
J2-L
J2-B
AXIS LOCATE GATE
J100-H
XMD
YMD
S/H J20-1
J8-13
J100-A
S/H J20-3
J8-21
J100-B
X DEPTH'
J100-C
Y DEPTH'
J100-F
DIV. DEPTH'
+5V
PERSP D/A
J100-B
YVP
XVP
J100-A CHR X POS
J100-B CHR Y POS
+5Y
CAESAR CPU

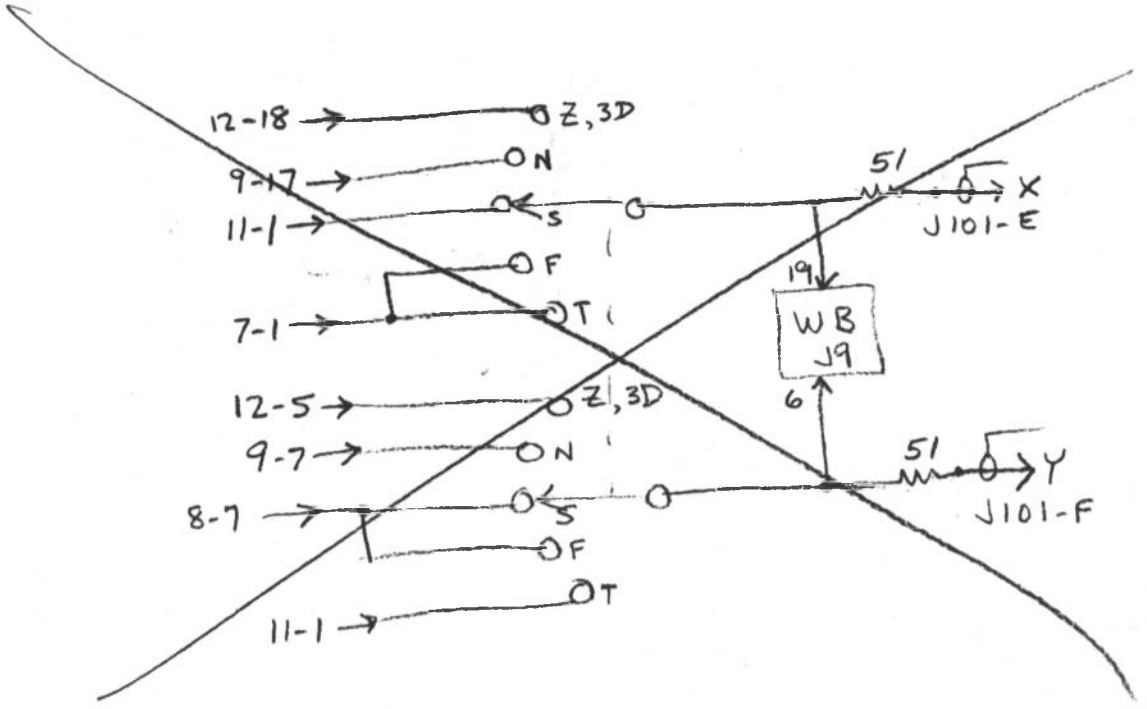



MODE SWITCH POSITIONS

1- NORM
2- ZOOM
3- 3D
4- TOP
5- FRONT
6- SIDE

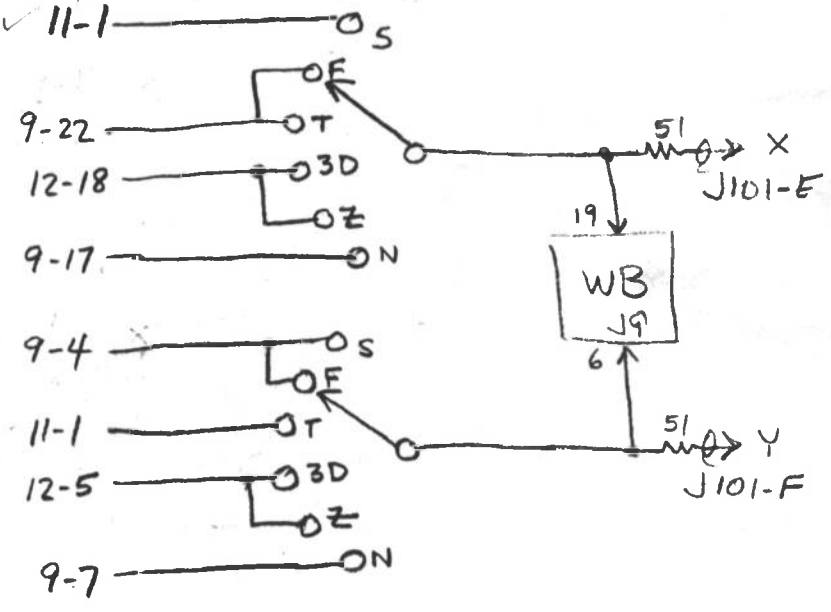
(4-6: 3D VIEWS)

CAESAR CPU

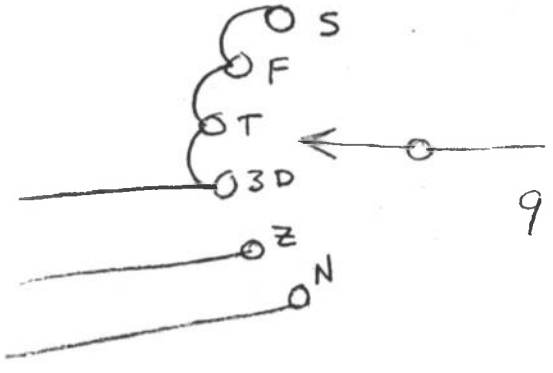



OLD

New 11 pole, 6 pos switch




PRESENT




9 other sections

CALSAR CPU

+10V
−10V

R1 10K
R2 10K
R3 10K
R4 10K
R5 10K
R6 10K
R7 10K
R8 10K
R9 10K
R10 10K
R11 10K
R12 10K

DEPTH OSC. → MM
VERT OSC. → NN
HORIZ OSC → PP
BLANKING STOP → S
BLANKING START → R
INTENSITY → P
DEPTH → C (F)
VERT AXIS → L
HORIZ AXIS → K
VERT SIZE → N
HORIZ SIZE → M
Y POS → E
X POS → D
OVERALL Y POS → B
OVERALL X POS → A

+15V → VV
GRD → WW, XX
−15V → UU

C3 10pf
R18 10K 1%
R19 10K
R15 10K 1%
10K
IC 1 1439G
R16 10K
COS
R17 390Ω
C4 .002µf
−15V
COS R → J

1µf 25V
+10V
−10V
GRD
+E COS
−E SIN
GRD
SIN-COS POT
1µf 25V

C5 10pf
R23 10K 1%
R20 10K 1%
10K
IC 2 1439G
R21 10K
R22 390Ω
C6 .002µf
SIN .002µf
−15 V
SIN R → H

HOR. RESET → W
VERT. RESET → V

J100

2N3568

+15V
R13 75Ω 1W 430
IN3064
+10V
30ma
D1 10V
C1 .1µf

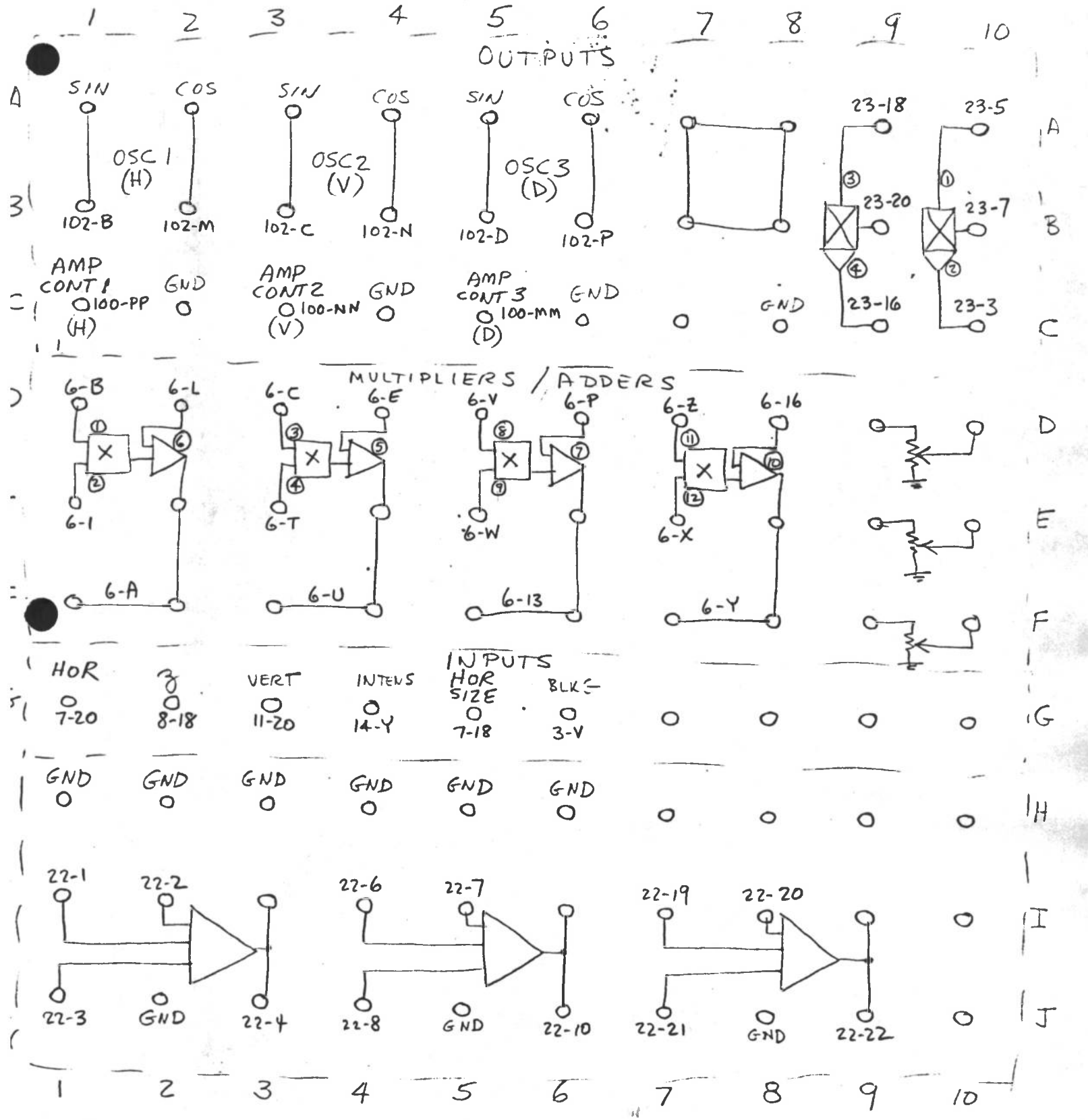
−15V
R14 75Ω 1W 430
2N3638 IN3064
−10V
30ma
D2 10V IN962B
C2 .1µf

S1 AXIS LOCATE ENABLE → JJ
S2 SHORT RAMP ENABLE (SECTION BLANKING) → T
S3 OVERLAP ENABLE (UP-DOWN) → AA
S4 SPARE (RIGHT-LEFT) → BB

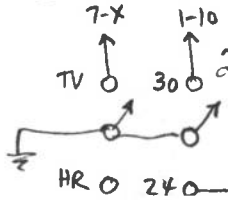
COMPUTER IMAGE CORPORATION
2475 W. 2nd AVE. DENVER, COLORADO 80223

| SCALE | NONE | REVISION | BY | DATE |
|---|---|---|---|---|
| DATE | 10-13-71 | | | |
| DR'N. E.R. | CK'D. | | | |
| APP'VD. | | | | |

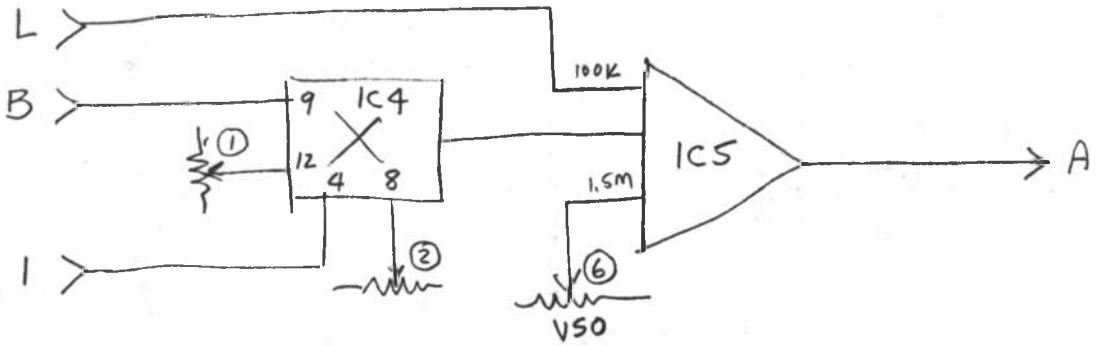
TITLE: CAESAR CPU FRONT PANEL SCHEMATIC
NO. CPUW-101

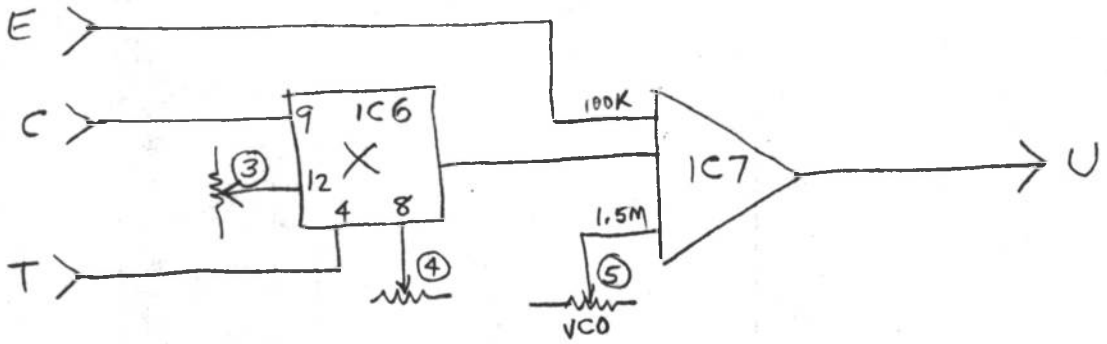


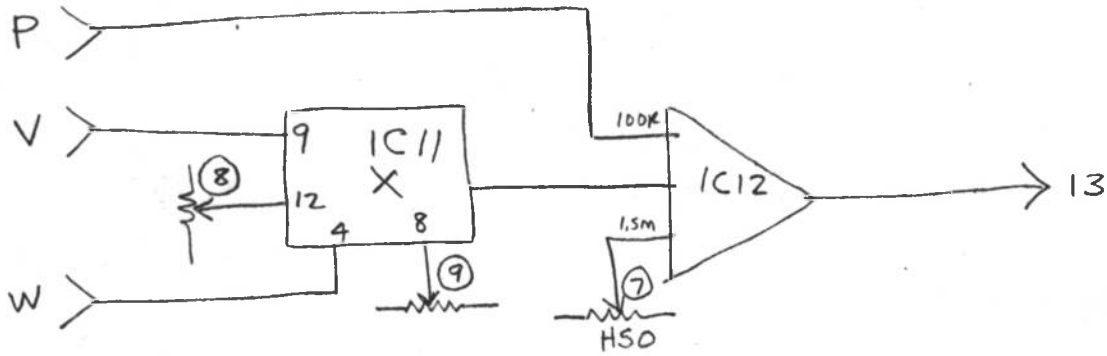

NOTE: 1. UNUSED INPUTS MUST BE GROUNDED EXCEPT BLANKING (G6)

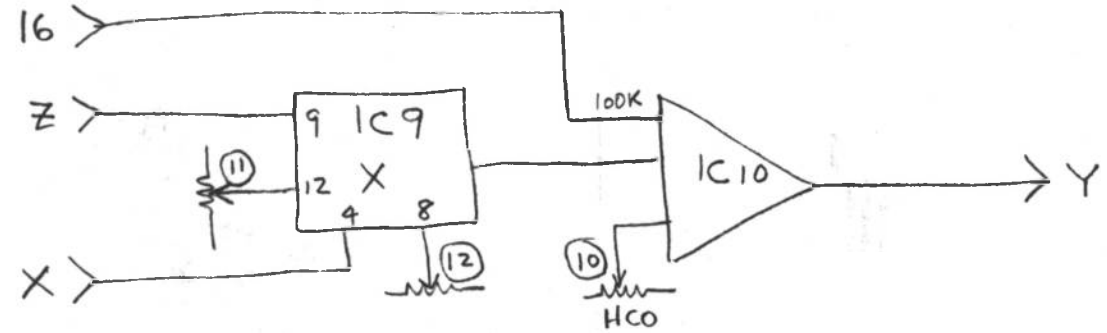


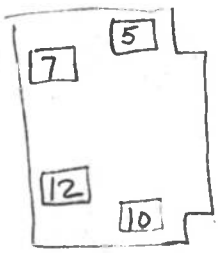

2. DO NOT CONNECT OUTPUTS TOGETHER



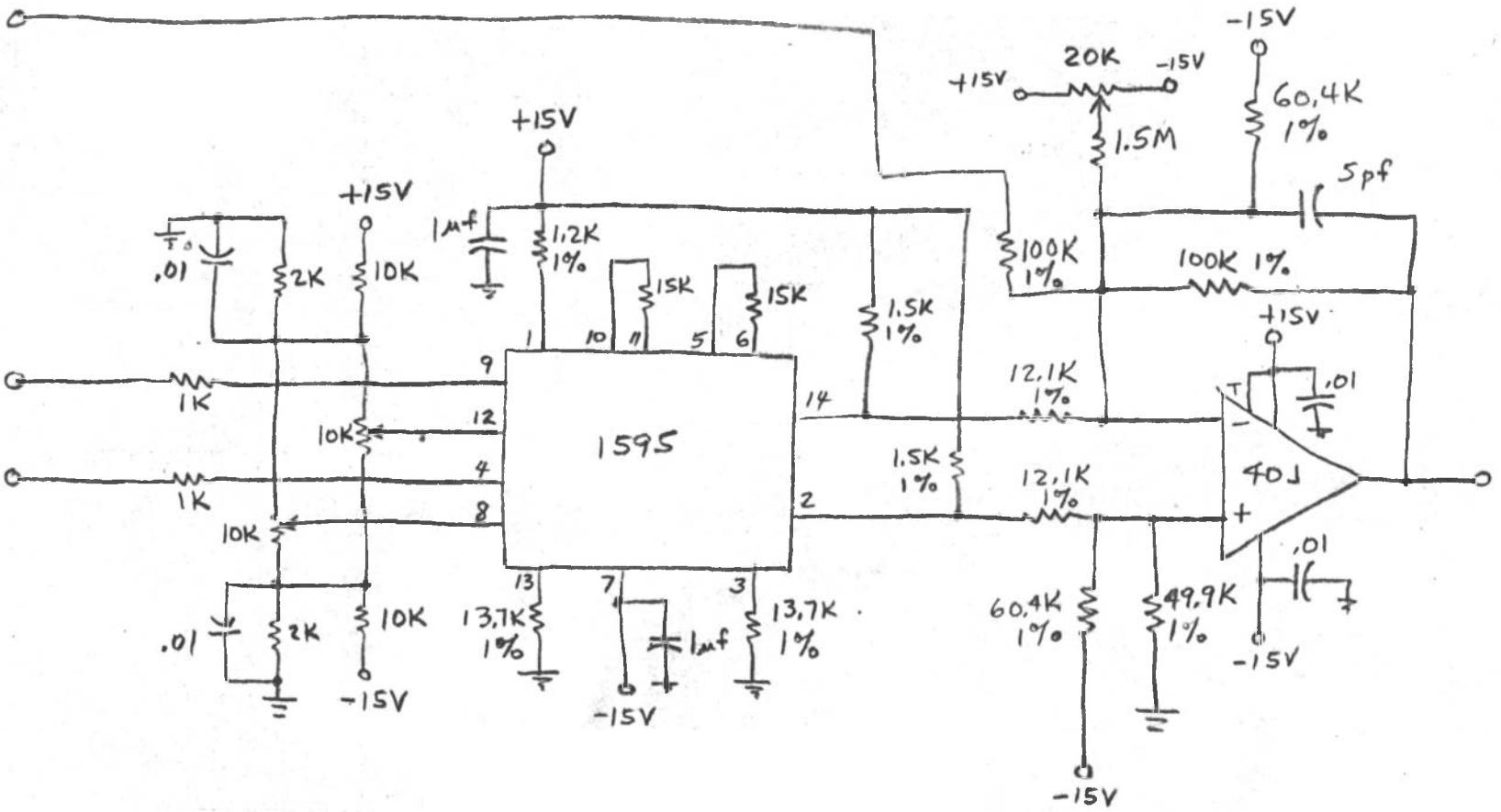




CAESAR CPU

SM-136

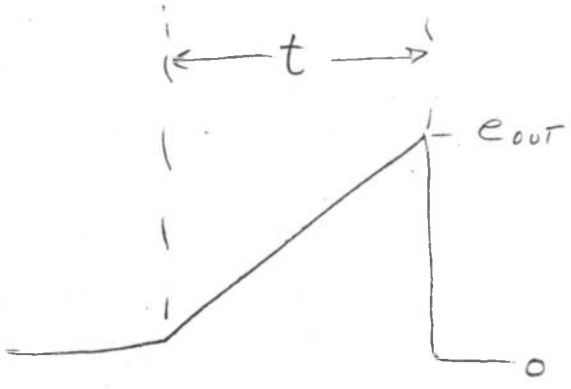
J6

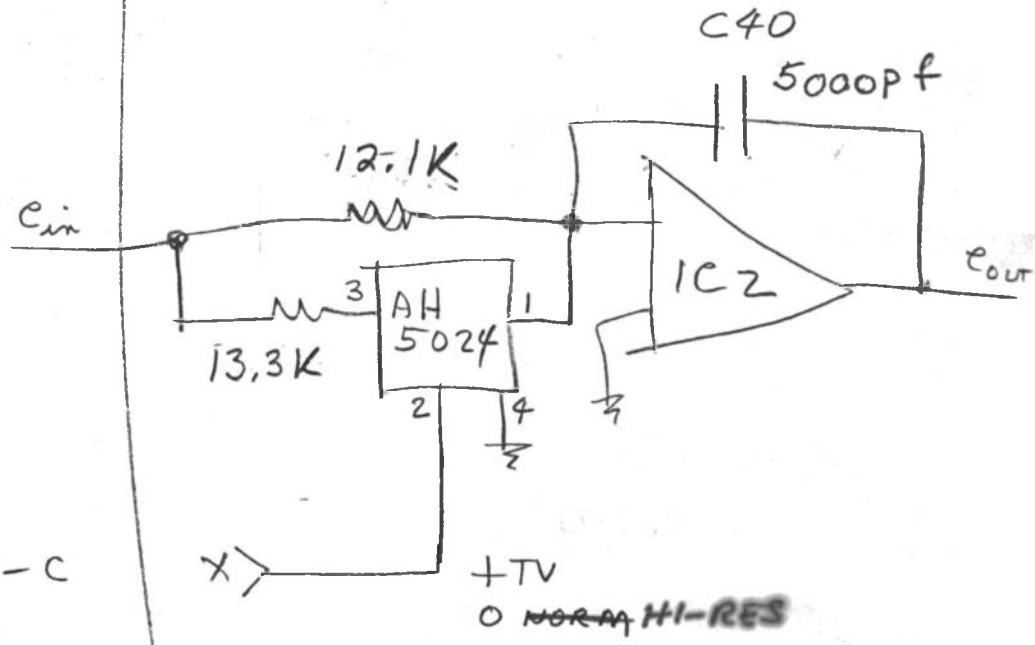



SM-136 (TYPICAL)

J6

| | ~~NORM~~ | TV |
|---|---|---|
| $t$ | 31.5 μS | 60 μS |
| $R$ | 6.336K | 12.1K |
| $C$ | 5000 pf | 5000 pf |
| $e_{in}$ | 10 V | 10 V |
| $\frac{iT}{C} = e_{OUT}$ | 9.94 V | 9.92 V |
| $i_{in}$ | 1.578 ma | .8264 ma |




H. Ramp.

TV RATES MOD. TO CPU-106

J7

T VERT/HORIZ IN
16 SINE R IN
18 HORIZ/VERT SIZE IN
17 DEPTH ANIM. IN
5 HORIZ/VERT RESET IN
3 X/Y POS IN
7 HORIZ/VERT SIZE IN
22 HORIZ/VERT AXIS IN
20 HORIZ/VERT ANIM IN
19
2 AXIS LOCATE IN
F HORIZ/VERT IN
4 COS R IN
14 +15V
11,12 GRD
9 -15V

V RC 16.7MS R8 178K C40 0.1µf
H 32MS 3.92K 8200pf

IC 1 8007C LF356
IC 2 40J
IC 3 MC1495L 1595
IC 4 40J
IC 5 8007C 40J
IC 6 MC1495L 1595
IC 7 40J
IC 8 8007C
IC 9 MC1495L 1595
IC 11 8007C

Q1 2N5133
Q2 2N4916
Q3 MEM517C
Q4 2N3644
Q5 2N3569
Q6 2N5462
Q7 2N5134
Q8 2N4351
TD101

D1 IN3064
D2 IN3064

SIN OFFSET
SIZE 2 OFFSET
AXIS dc OFFSET
AXIS X OFFSET
AXIS Y OFFSET
SIZE 1 OFFSET
COS OFFSET

J7(H) ONLY
J11(VERT) ONLY
H: NE5534
V: 40J
NEW CIRC.

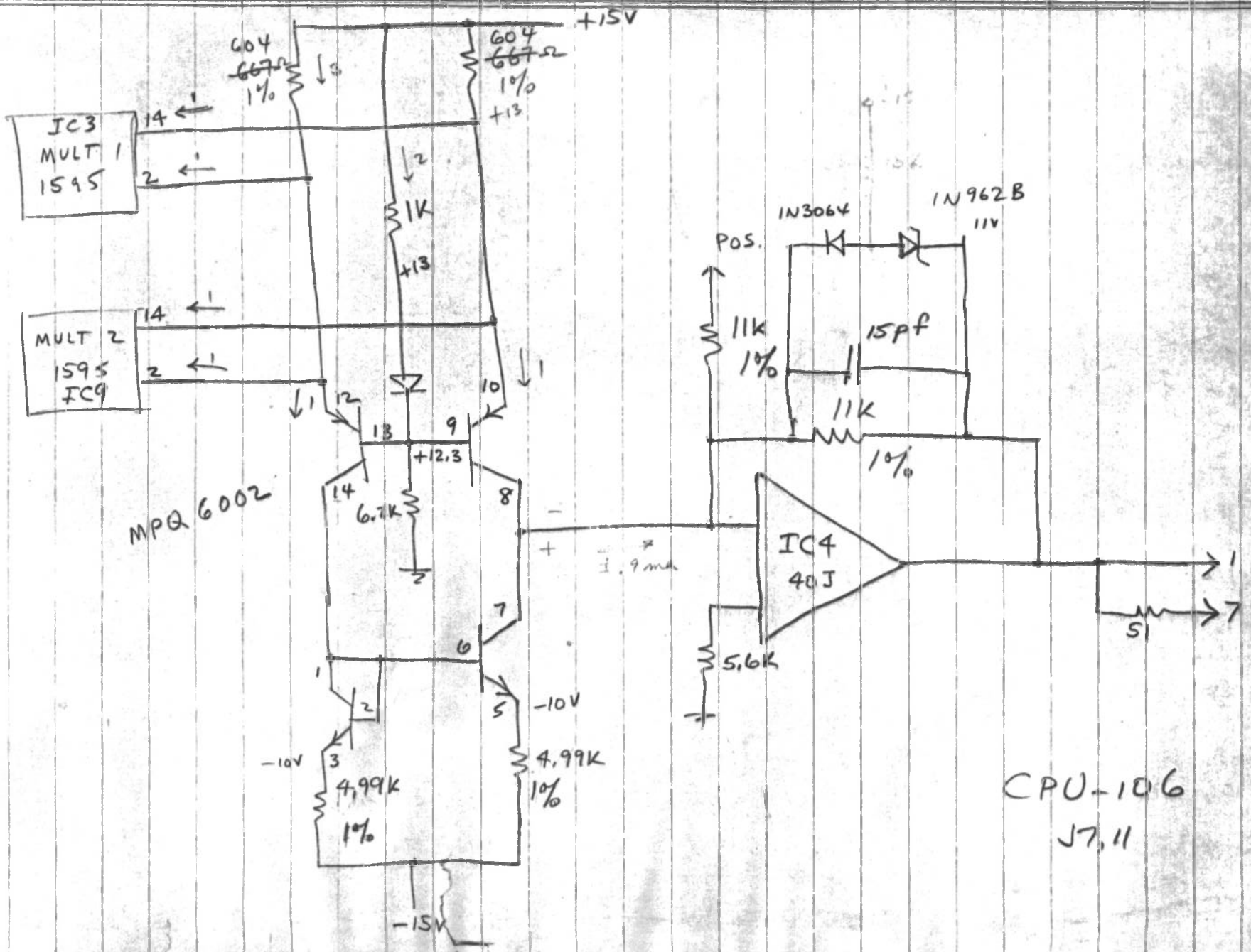
X/Y OUT
HORIZ/VERT OUT
HORIZ/VERT SIZE OUT
AXIS X SIZE OUT
HORIZ/VERT ANIM. OUT

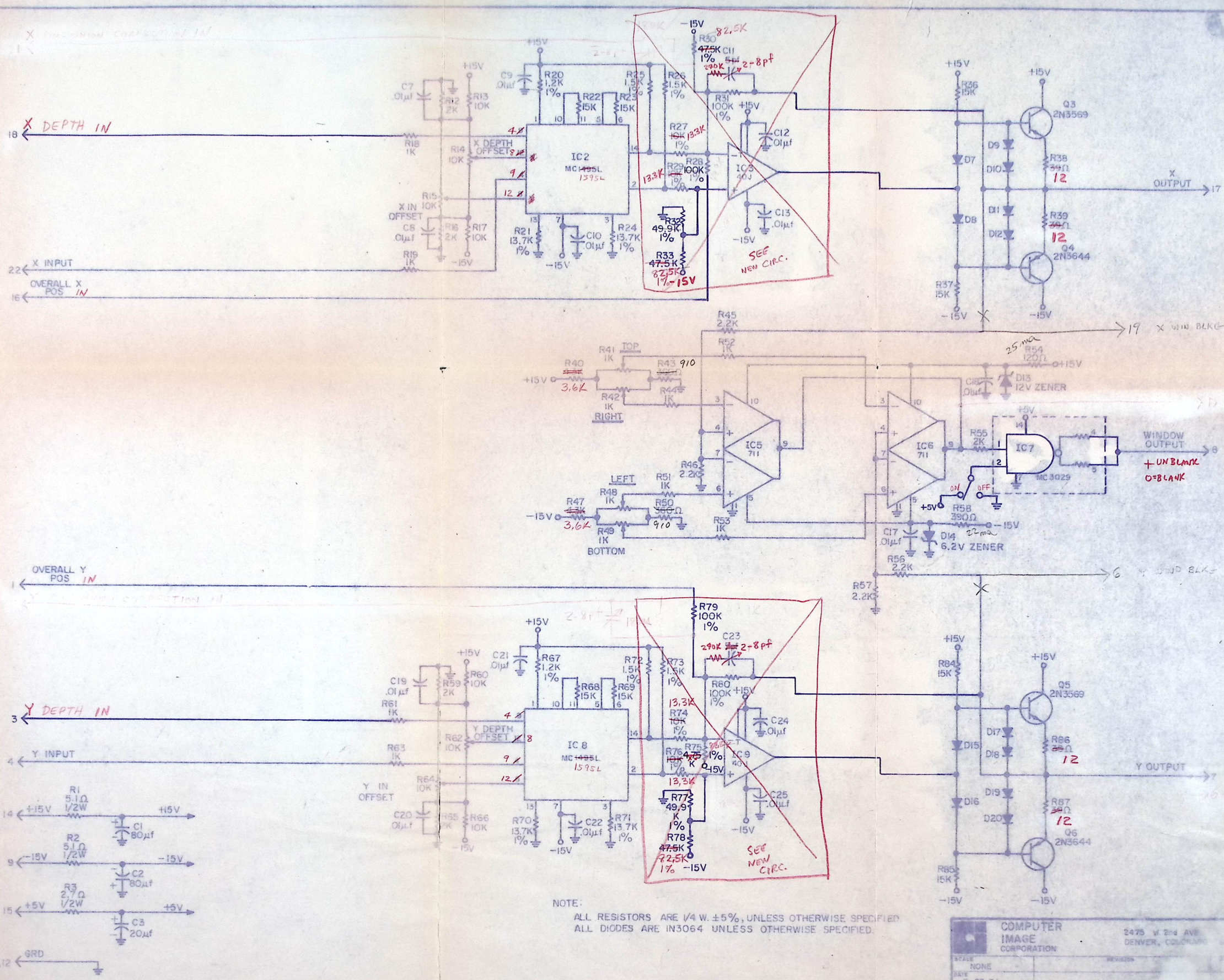
GATE

J7 - X
J11 - Y

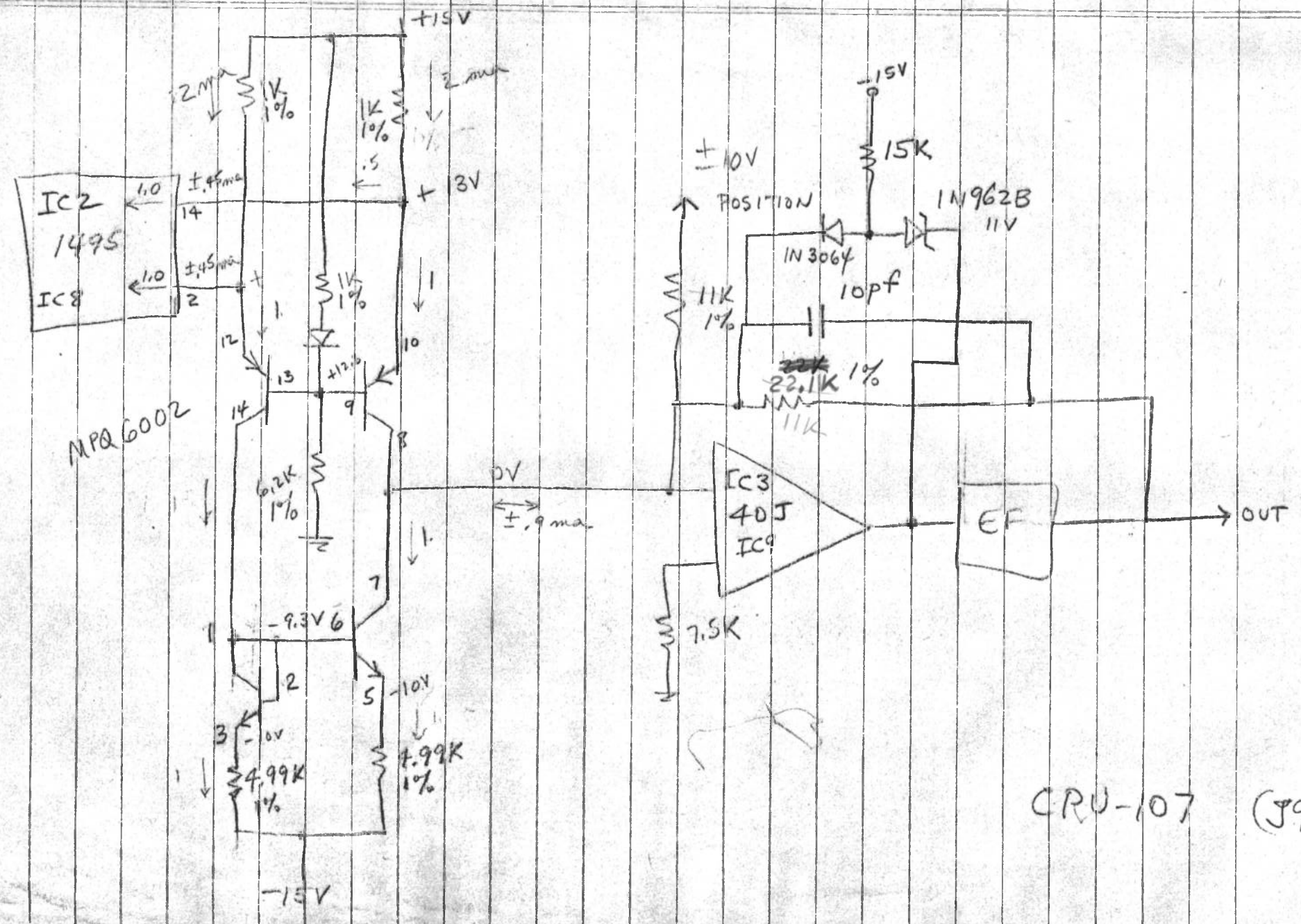
NOTE
* INDICATES SELECTED VALUE

| | | | |
|---|---|---|---|
| COMPUTER IMAGE CORPORATION | 2475 W. 2nd. AVE. DENVER, COLORADO 80223. | | |
| SCALE NONE | REVISION REV. A | BY E.R. | DATE 10-4-71 |
| DATE 6-22-71 | | | |
| DR'N. E.R. CK'D. | | | |
| APP'VD. | | | |
| TITLE X/Y CHANNEL | J7, J11 | NO. CPU-106A | |


+15V
604 667Ω 1%
604 667Ω 1%
IC3 MULT 1 1595
14
2
1K
+13
MULT 2 1595 IC9
12
13
9
10
+12.3
MPQ 6002
14
6.7K
8
7
6
5
-10V
1
2
3
4,99K 1%
4,99K 1%
-15V
IN3064
IN962B 11V
POS.
11K 1%
15pf
11K 1%
IC4 40J
5.6K
51
CPU-106
J7,11

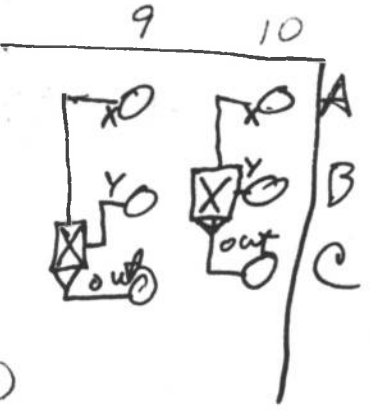


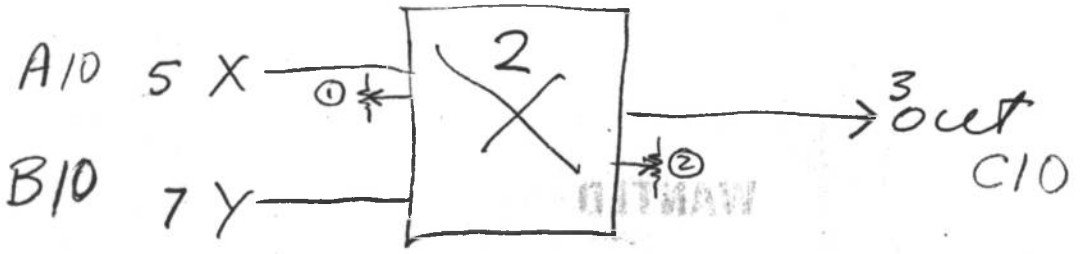

COMPUTER IMAGE CORPORATION
2475 W. 2nd AVE. DENVER, COLORADO
SCALE NONE
DATE 6-25-71
DRWN E.R.
CHKD
APVD
REVISION
TITLE DEPTH & OUTPUT SECTION
CAESAR
J9
CPU-107

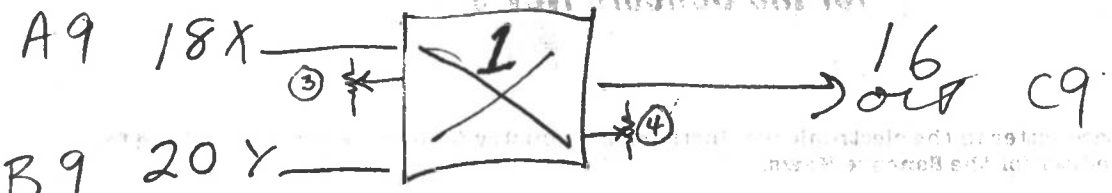

+15V
2 ma
1K 1%
1K 1%
.5
+ 3V
IC2
1495
IC8
1.0
±.45ma
14
2
12
13
10
9
8
7
6
5
3
1
MPQ6002
6.2K 1%
-9.3V
-10V
-0V
4.99K 1%
4.99K 1%
-15V
0V
±.9 ma
±10V
POSITION
-15V
15K
1N962B
11V
1N3064
10pf
11K 1%
22.1K 1%
11K
IC3
40J
IC9
7.5K
EF
OUT
CRU-107 (J9)

~~J25~~ J23

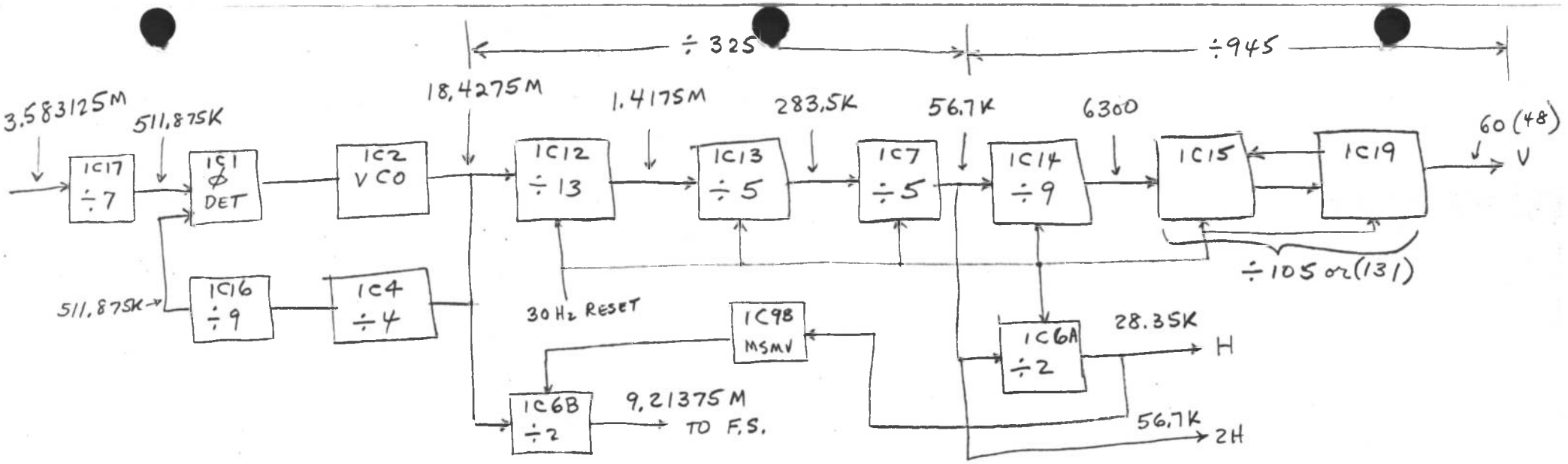
# AM-107



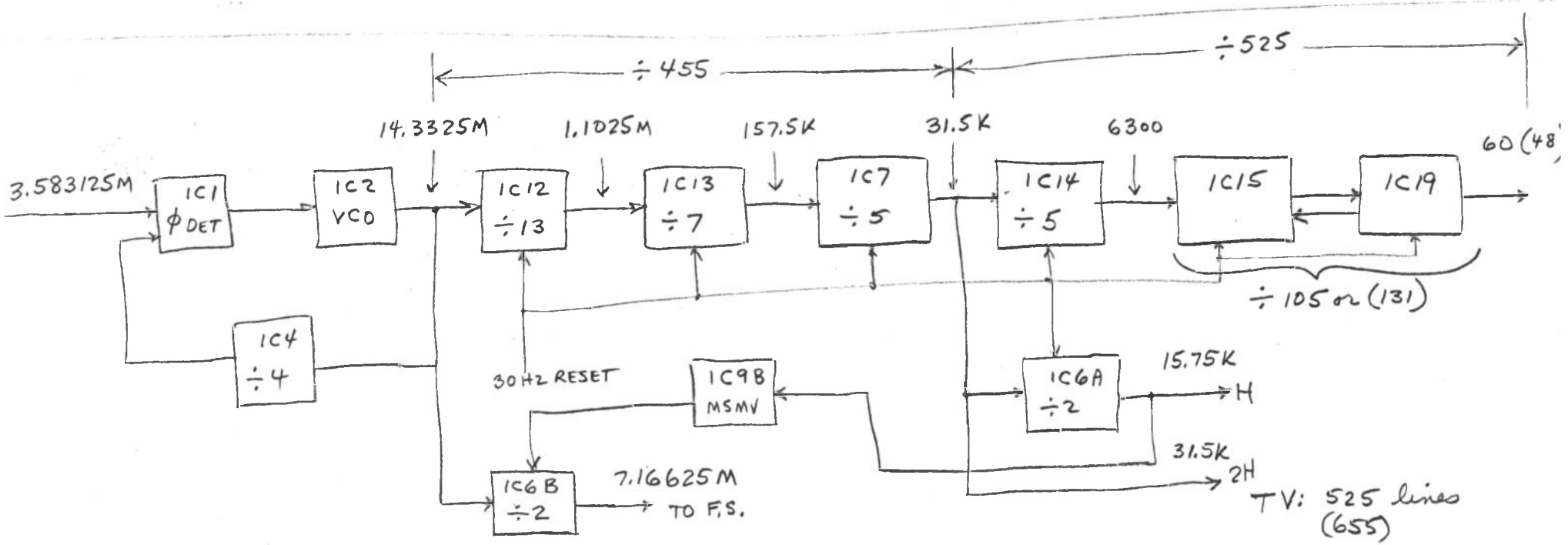




50K Pots



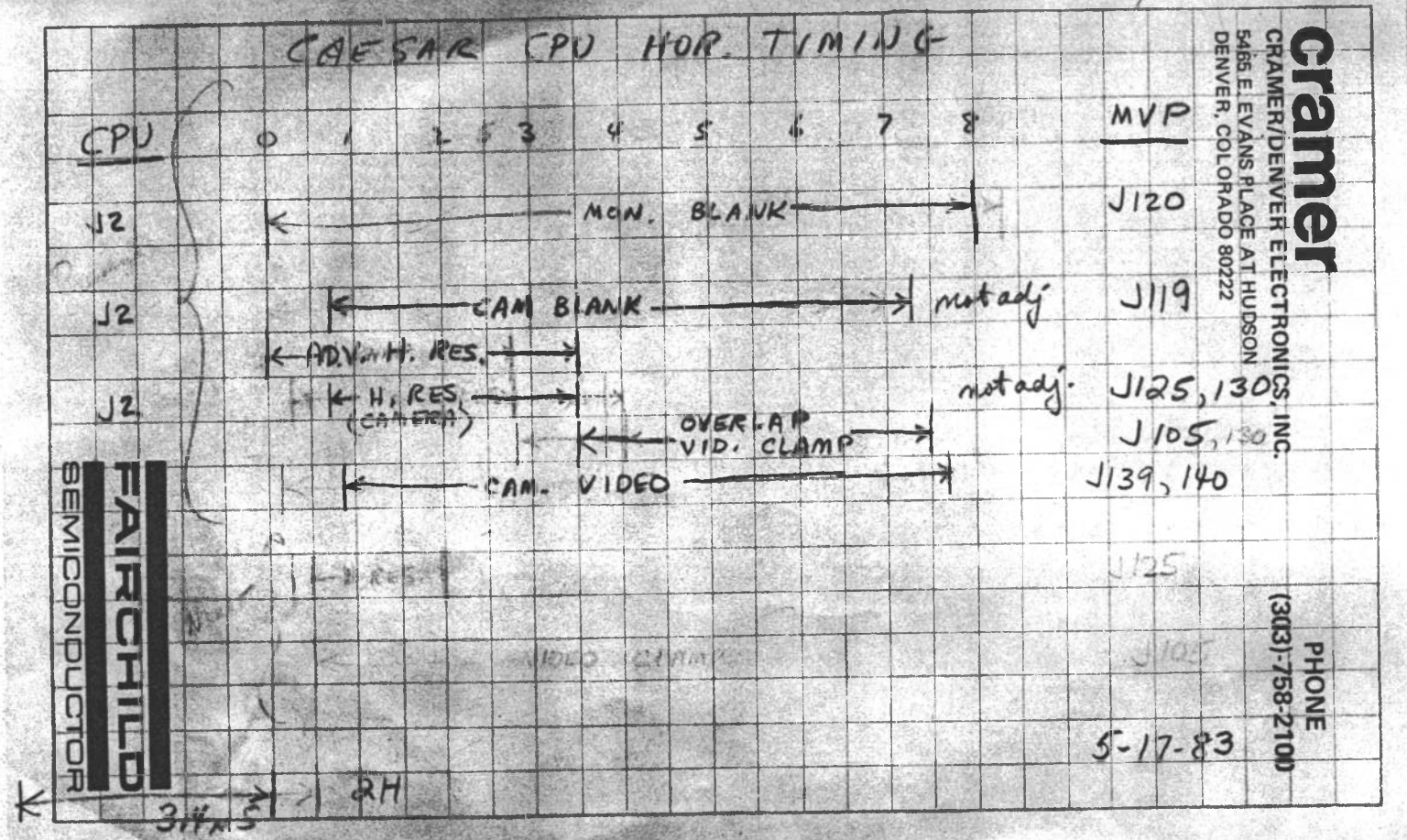

HI RES: 945 lines
(1179)

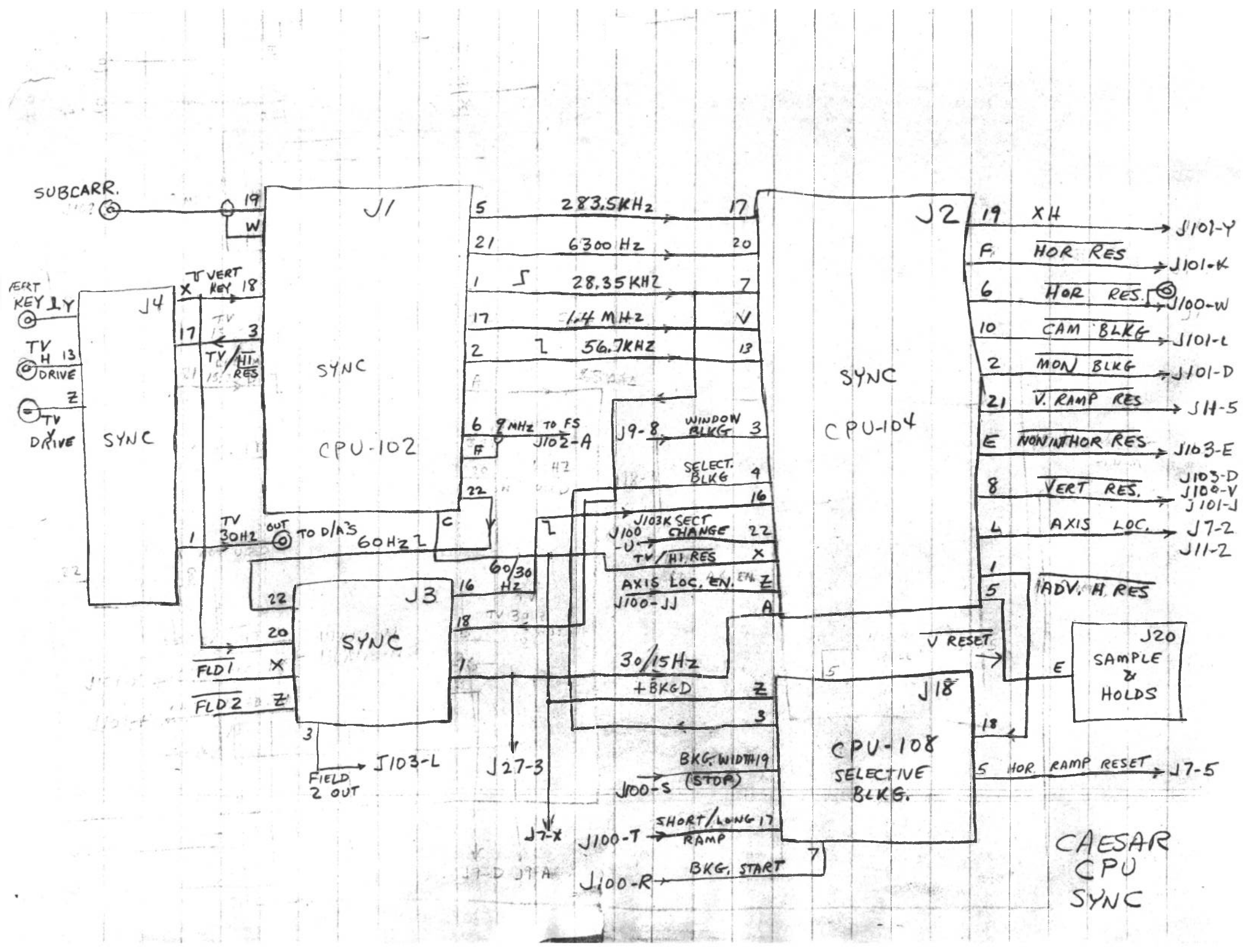


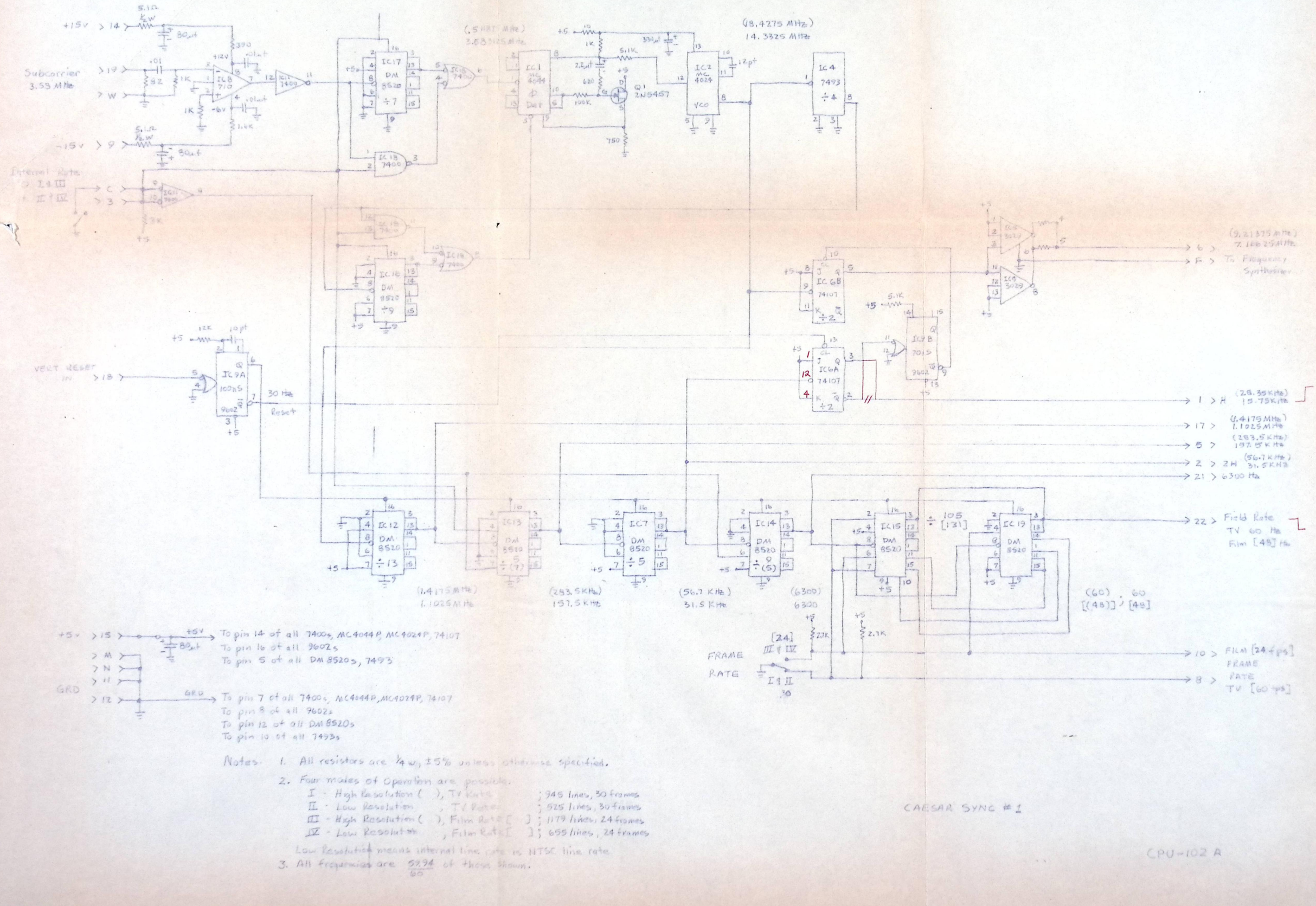

TV: 525 lines
(655)

ALL FREQ. $\frac{59.94}{60}$ × THOSE SHOWN

CAESAR CPU J1


CAESAR CPU HOR. TIMING
CPU
0 1 2 3 4 5 6 7 8
MVP
J2
MON. BLANK
J120
J2
CAM BLANK
not adj
J119
ADV. H. RES.
J2
H. RES (CAMERA)
not adj.
J125, 130
OVERLAP VID. CLAMP
J105, 130
CAM. VIDEO
J139, 140
J125
5-17-83
cramer
CRAMER/DENVER ELECTRONICS, INC.
5465 E. EVANS PLACE AT HUDSON
DENVER, COLORADO 80222
PHONE
(303)-758-2100
FAIRCHILD
SEMICONDUCTOR


SUBCARR.
J1
SYNC
CPU-102
J4
SYNC
J3
SYNC
SYNC
CPU-104
J2
283.5KHz
6300 Hz
28.35KHz
1.4 MHz
56.7KHz
9 MHz TO FS
J102-A
WINDOW BLKG
SELECT. BLKG
J103K SECT CHANGE
TV/HI RES
AXIS LOC. EN.
J100-JJ
TV 30Hz OUT
TO D/A'S
60Hz
60/30 Hz
30/15Hz
+BKGD
FLD1
FLD2
FIELD 2 OUT
J103-L
J27-3
J7-X
BKG. WIDTH 19
J100-S (STOP)
SHORT/LONG 17 RAMP
J100-T
BKG. START
J100-R
J18
CPU-108
SELECTIVE BLKG.
V RESET
ADV. H. RES
J20
SAMPLE & HOLDS
HOR. RAMP RESET
J7-5
XH
J101-Y
HOR RES
J101-K
HOR RES.
J100-W
CAM BLKG
J101-L
MON BLKG
J101-D
V. RAMP RES
J11-5
NONINTHOR RES
J103-E
VERT RES.
J103-D
J100-V
J101-J
AXIS LOC.
J7-2
J11-2
VERT KEY 1Y
TV H DRIVE
TV Y DRIVE
TV VERT KEY
TV/HI RES
CAESAR CPU SYNC

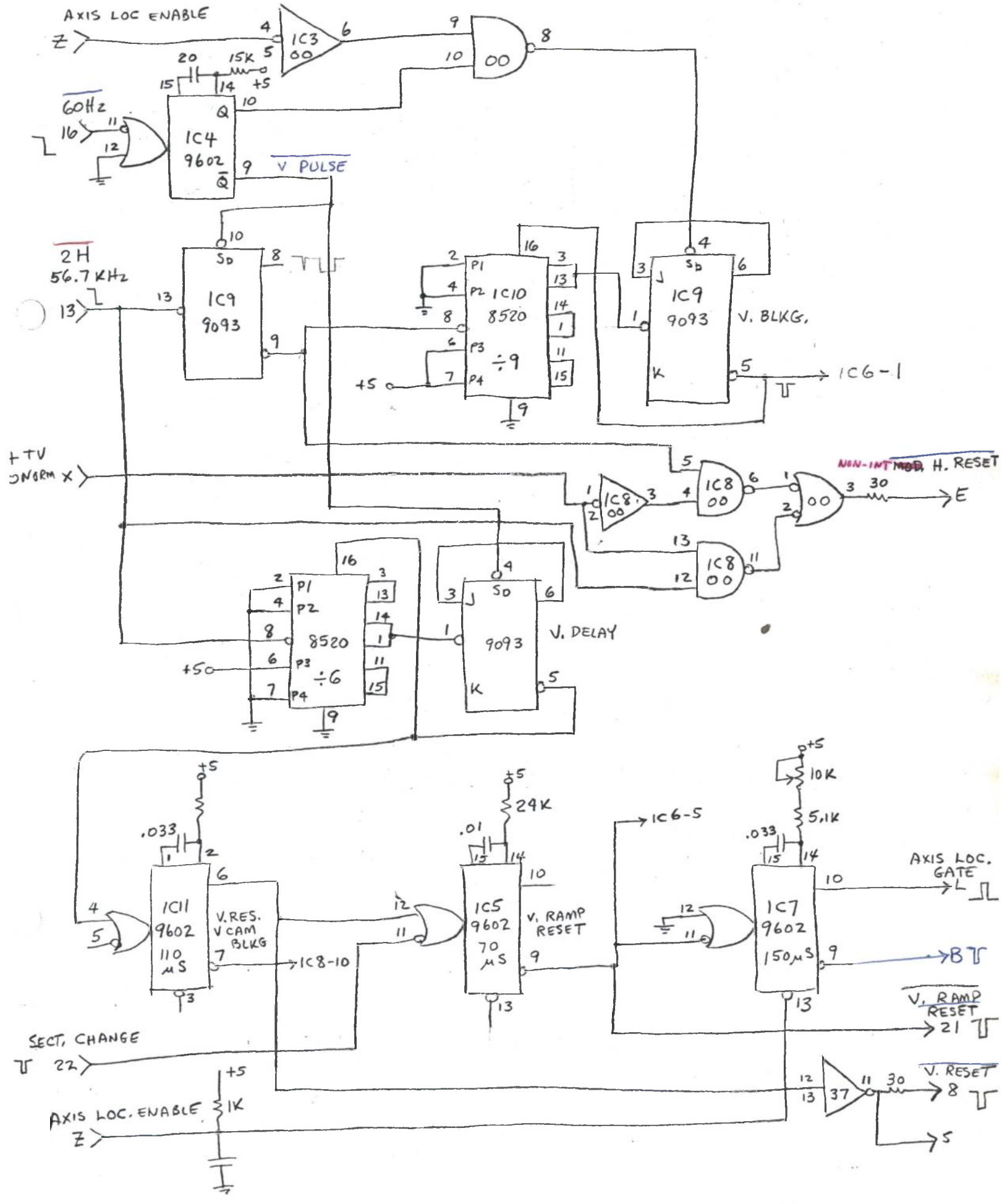



Notes:
1. All resistors are ¼ w, ±5% unless otherwise specified.
2. Four modes of Operation are possible:
   - I - High Resolution ( ), TV Rate ; 945 lines, 30 frames
   - II - Low Resolution , TV Rate ; 525 lines, 30 frames
   - III - High Resolution ( ), Film Rate [ ] ; 1179 lines, 24 frames
   - IV - Low Resolution , Film Rate [ ] ; 655 lines, 24 frames

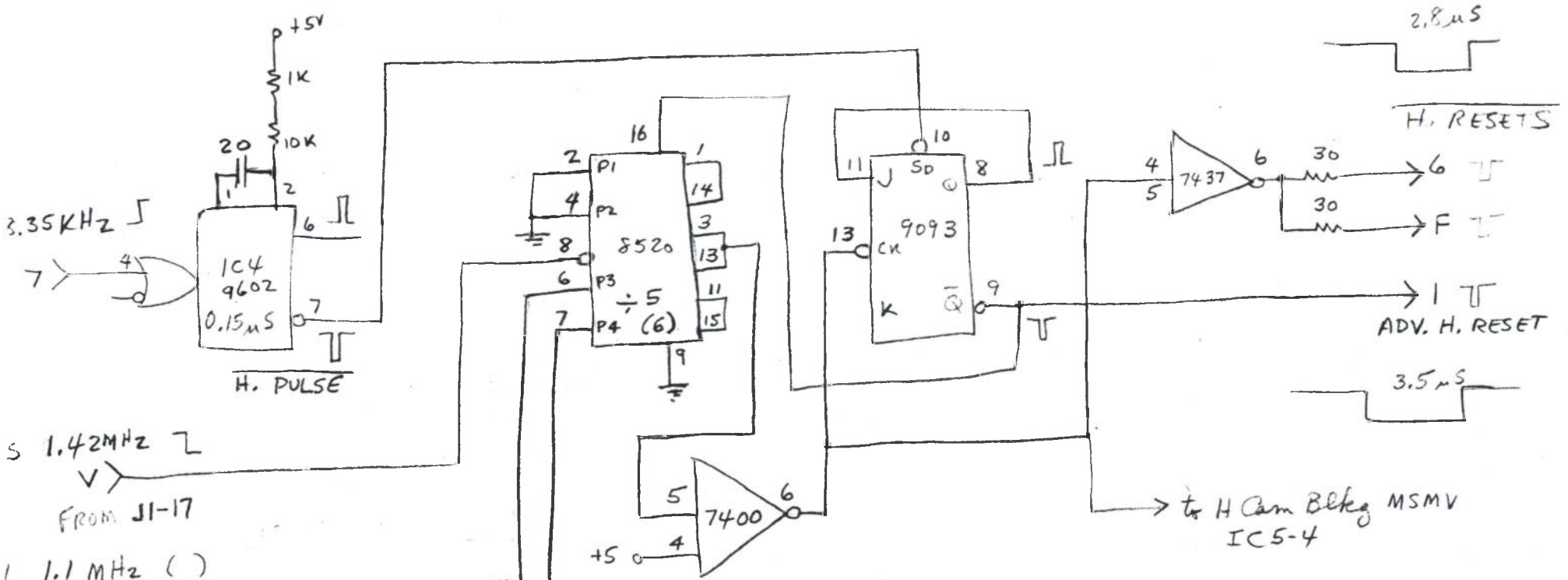
   Low Resolution means internal line rate is NTSC line rate.
3. All frequencies are $\frac{59.94}{60}$ of those shown.

CAESAR SYNC #1

CPU-102 A




PART OF CPU-104 (J2)



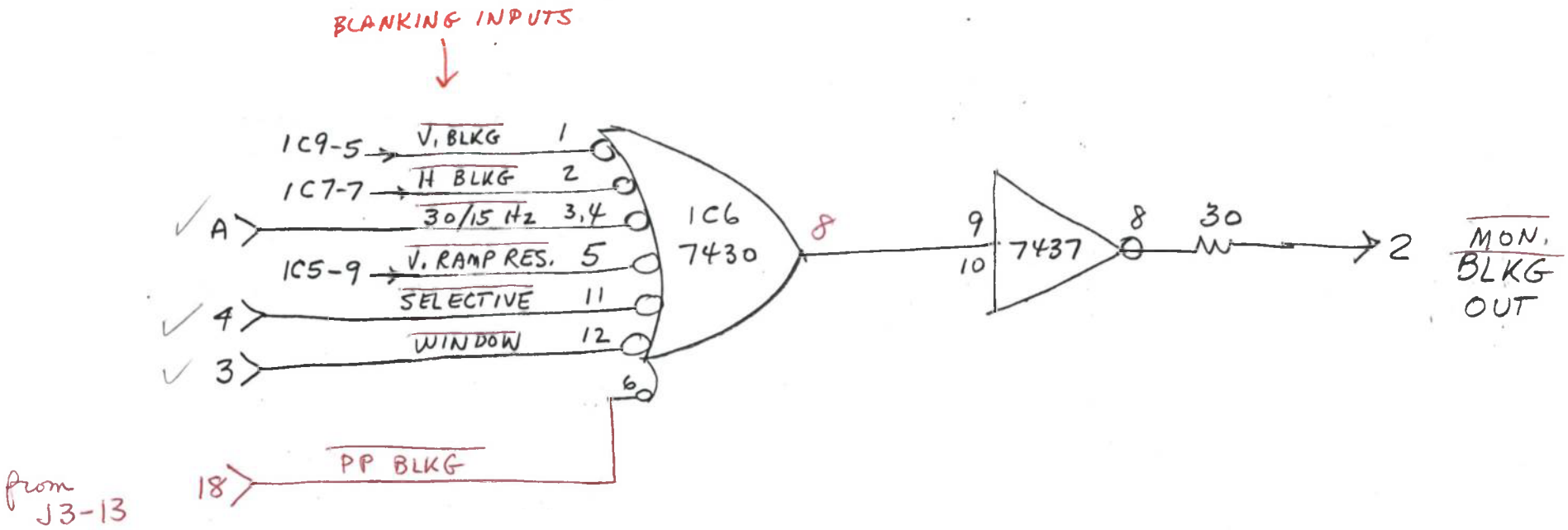

| | ADV. H | CAM. H |
|---|---|---|
| HI RES | 3.5 | 2.8 μS |
| LO RES | 5.4 | 4.5 |

5 6
0001 0010

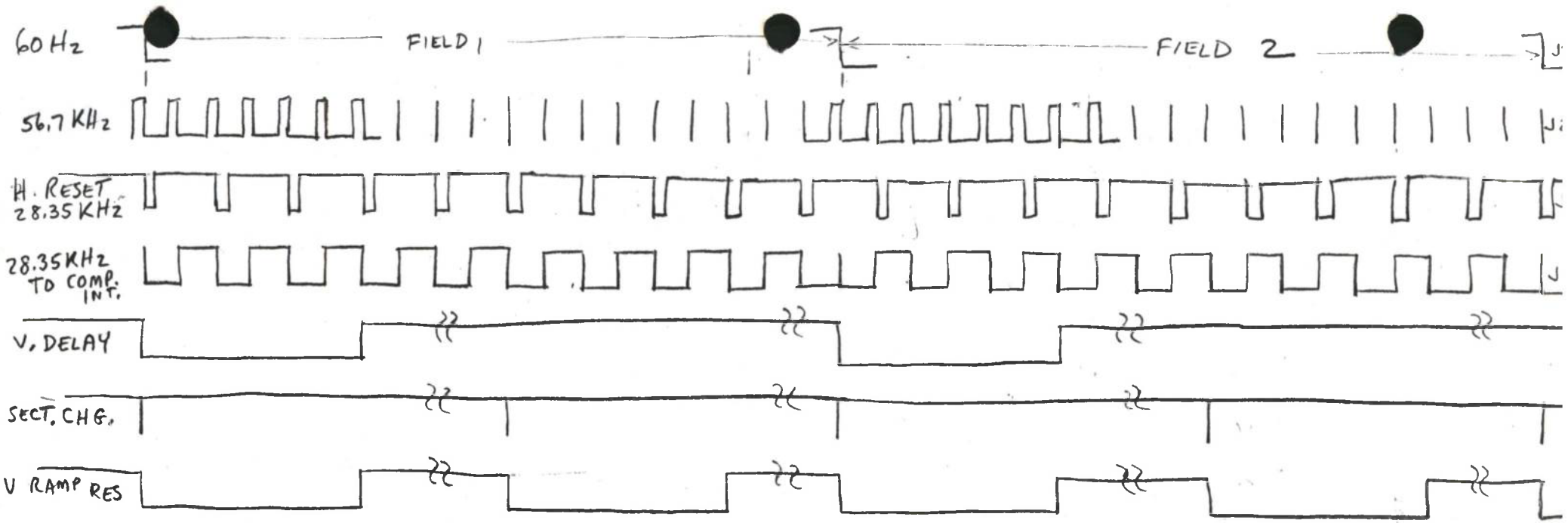
HORIZ. RESET GEN.

PART OF CPU-104

J2




PART OF CAESAR CPU-104
J2


60 Hz
FIELD 1
FIELD 2
56.7 KHz
H. RESET 28.35 KHz
28.35 KHz TO COMP. INT.
V. DELAY
SECT. CHG.
V RAMP RES

| | | HI-RES ~~NORM~~ | TV |
|---|---|---|---|
| V BLKG | CTR | 9L | 9L |
| V DEL | CTR | 3L | 3L |
| V RES | MSMV | 2L | 1L |
| AXIS LOC | MSMV | 4L | 2L |

17 ← 283.5KHz
VI 595.35 kHz
VN (604.9 kHz)
[604.8 kHz]

20 ← 6300 Hz
900 Hz
(900 Hz)
[720 Hz]

HORIZ. XH POSITION

VERT XH. POS.

IC 1A AM9602 · IC 1B AM9602 · IC 2B AM9602 · IC 2A AM9602

C2 .1µf · R2 5.1K · R3 20K · C3 .015µf · R4 5.1K · R5 1K 3K · C4 100pf · R6 15K · R7 20K · C5 10pf · R8 5.1K · R9 1K · +5V

1.42 MHz V

IC 3D 7400

IC 3 00 · IC 3 00 · 330 · CROSSHATCH OUT → 19

IC 3A 400 · R10 300Ω · CROSSHATCH OUT → 19

R11 300Ω · CROSSHATCH OUT → 18

3 ← WINDOW BLANKING IN

4 ← SELECTIVE BLANKING IN

FROM SEL. BLKG CARD SHT 3

D1 IN3064

30 · 30 · HORIZ RESET OUT → 6

7 ← 28.35 kHz (28.8 kHz) [28.8 kHz]

CAMERA BLANKIN OUT → 10

HORIZ BLANK

C8 1800pf · R18 10K · R19 5.6K · 6.6 µS · H. CAM. BLKG.

IC 5A AM9602 · IC 8C 7400 · Q2 2N5134 · R22 5.1K · R33 1K · +5V

C11 3000pf · R24 5.1K · R25 10K · 8µS · IC 7A AM9602

7437 · 3 · 30

9 · 10 · 7437 · 8 · 30 · R27 1K · MONITOR BLANKING OUT → 2 · Q3 2N5134 · R26 5.1K

IC 6 DM 930N 7410 · IC 6 7410 · IC 6 7410

VERT RAMP RESET OUT → 21

105 mS

VERTICAL BLANK

C15 .12µf · R38 5.1K · R39 10K · 350 mS · IC 7B AM9602

R41 1K · MONITOR VERT BLANKING OUT → 5 · Q6 2N5134

A · B · C · R40 5.1K · EYELETS

A 15/30HZ IN +BKGD. 0 ANIM.

IC 4A AM9602 · IC 4B AM9602

C6 20pf · R12 10K · R13 1K · C7 680pf · R15 10K · R14 10K · H. RES · Q1 2N5134 · R16 5.1K · R17 1K

from H Reset circuit

7437

HOR. RESET

60 Hz (60 Hz) [48 Hz] ← 16

CHANGE SECTION LENGTH IN ← 22

C12 300pf · R28 5.6K · R29 5.6K

56.7 kHz (57.6 kHz) [57.6 kHz] ← 13

IC 9D 7400 · IC 8D 7400 · IC 8B 7400 · IC 8A 7400 · IC 9B 9093 · IC 10 DM 8520 ÷4,5 · IC 9A 9093

TVN F · TV I · +5V

R42 5.6K · C15 .01µf · R43 5.6K · 1K

LOCATOR AXIS ENABLE

R31 1K · Q4 2N5134 · R30 1K

÷6

54K · .01µf

21 VERT RAMP RESET OUT

C9 300pf · C10 .03µf · R20 10K · R21 12K · 12K

C13 .03µf · R33 1.6K · R32 3.1K · V. CAM BLKG. 130 mS

IC 5B AM9602 · IC 11B AM9602 · V. RES DELAY 1.5 µS

C14 .03µf · R34 10K · 12K · R35 1K 510 · IC 11A AM9602 · 40 mS · V. RES. 115 mS

R36 5.1K · Q5 2N5134 · R37 1K · VERT. RESET OUT → 8

30 · 30 · 7437

15 ← +5V RI JUMPER · C1 80µf · 11 ← GRD · 12 ← GRD

POSITIVE BLANK (BLANKING) ANS LOCATOR

TO PIN 14 OF ALL DM8000's, 930, 9[illegible] 7410
TO PIN 16 OF ALL AM9602's
TO PIN 5 OF DM 8520

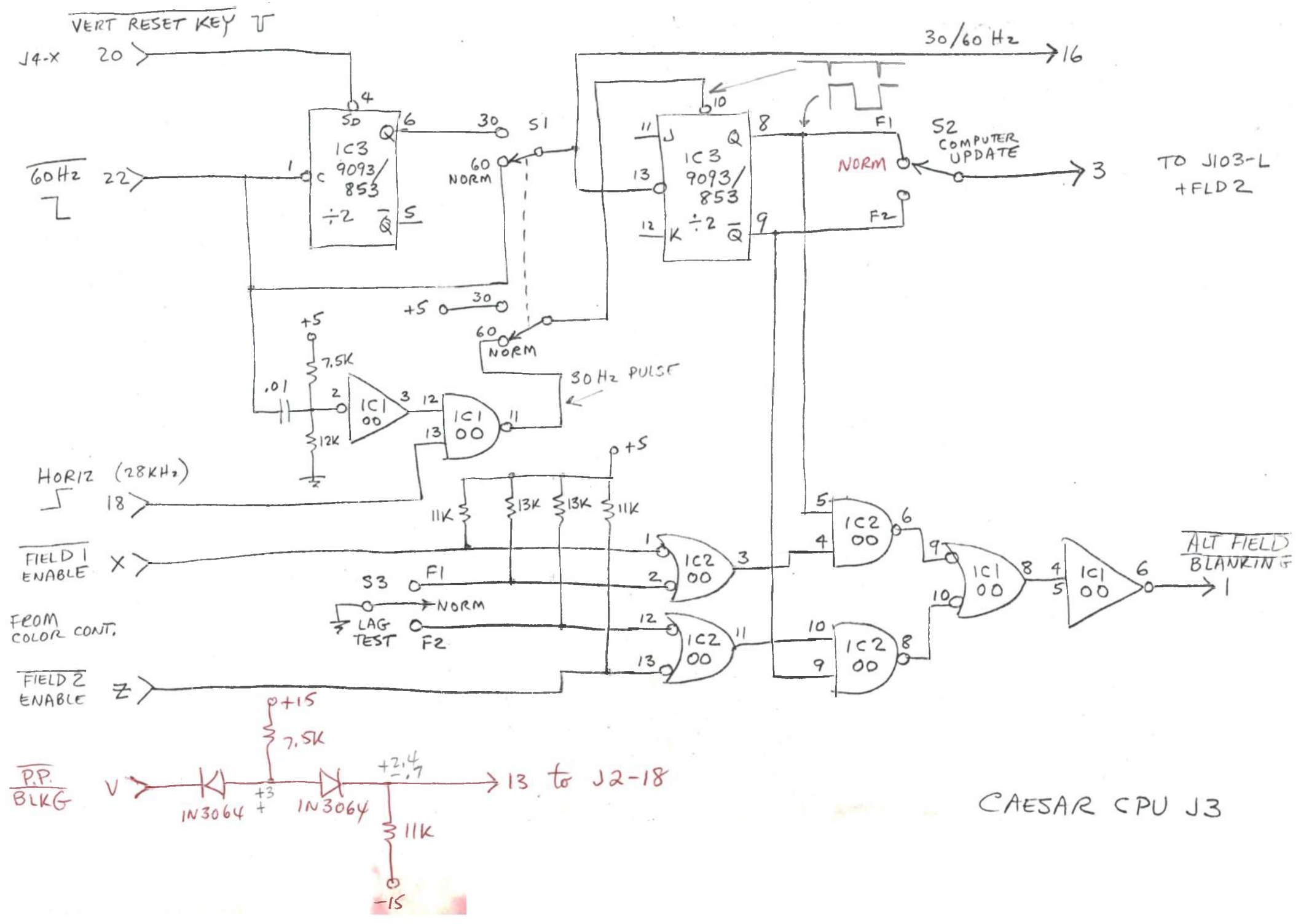
TO PIN 7 OF ALL DM 8000's, 930, 9[illegible]
TO PIN 8 OF ALL AM 9602's
TO PIN 12 OF DM 8520

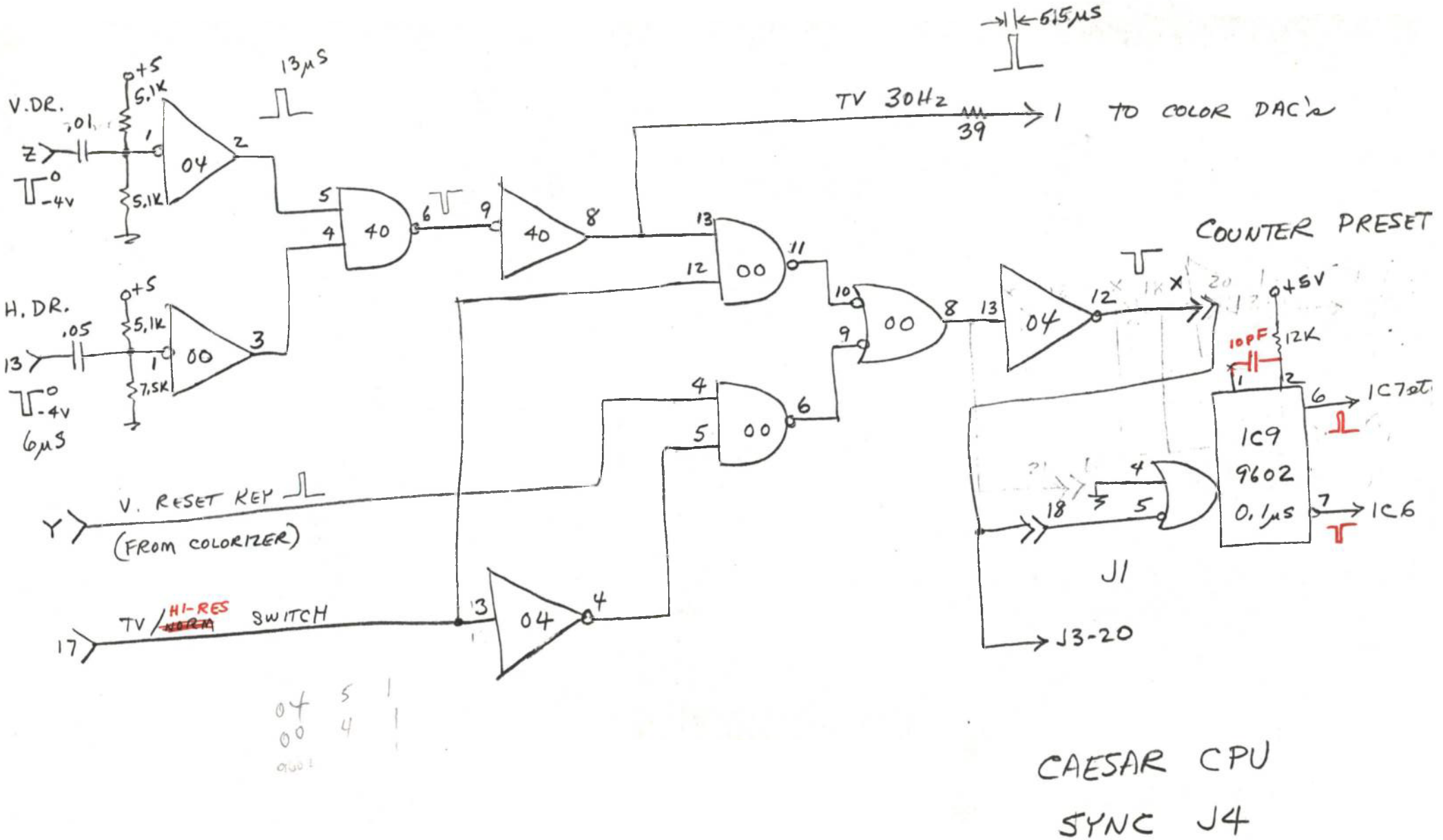
÷4

NOTES
1. * INDICATES TEMPERATURE STABLE CAPACITORS.
2. ALL RESISTORS ARE 1/4W. ± 5%, UNLESS OTHERWISE SPECIFIED.

COMPUTER IMAGE CORPORATION
2475 W. 2nd AVE.
DENVER, COLORADO 80223

| | | | |
|---|---|---|---|
| SCALE | NONE | REVISION | BY / DATE |
| DATE | 1-19-71 | | |
| DR'N | E.R. | CK'D. | |
| APP'VD. | | | |
| TITLE | CAESAR SYNC #2 | NO. | CPU-104 |


VERT RESET KEY
J4-X 20
30/60 Hz
16
IC3 9093/853
÷2
60Hz 22
S1
S2 COMPUTER UPDATE
NORM
TO J103-L +FLD 2
F1
F2
+5
7.5K
.01
12K
IC1 00
30 Hz PULSE
HORIZ (28KHz) 18
11K
13K
13K
11K
IC2 00
FIELD 1 ENABLE X
S3
LAG TEST
FROM COLOR CONT.
FIELD 2 ENABLE Z
ALT FIELD BLANKING 1
+15
-15
P.P. BLKG V
IN3064
+2.4 ±.7
13 to J2-18
CAESAR CPU J3

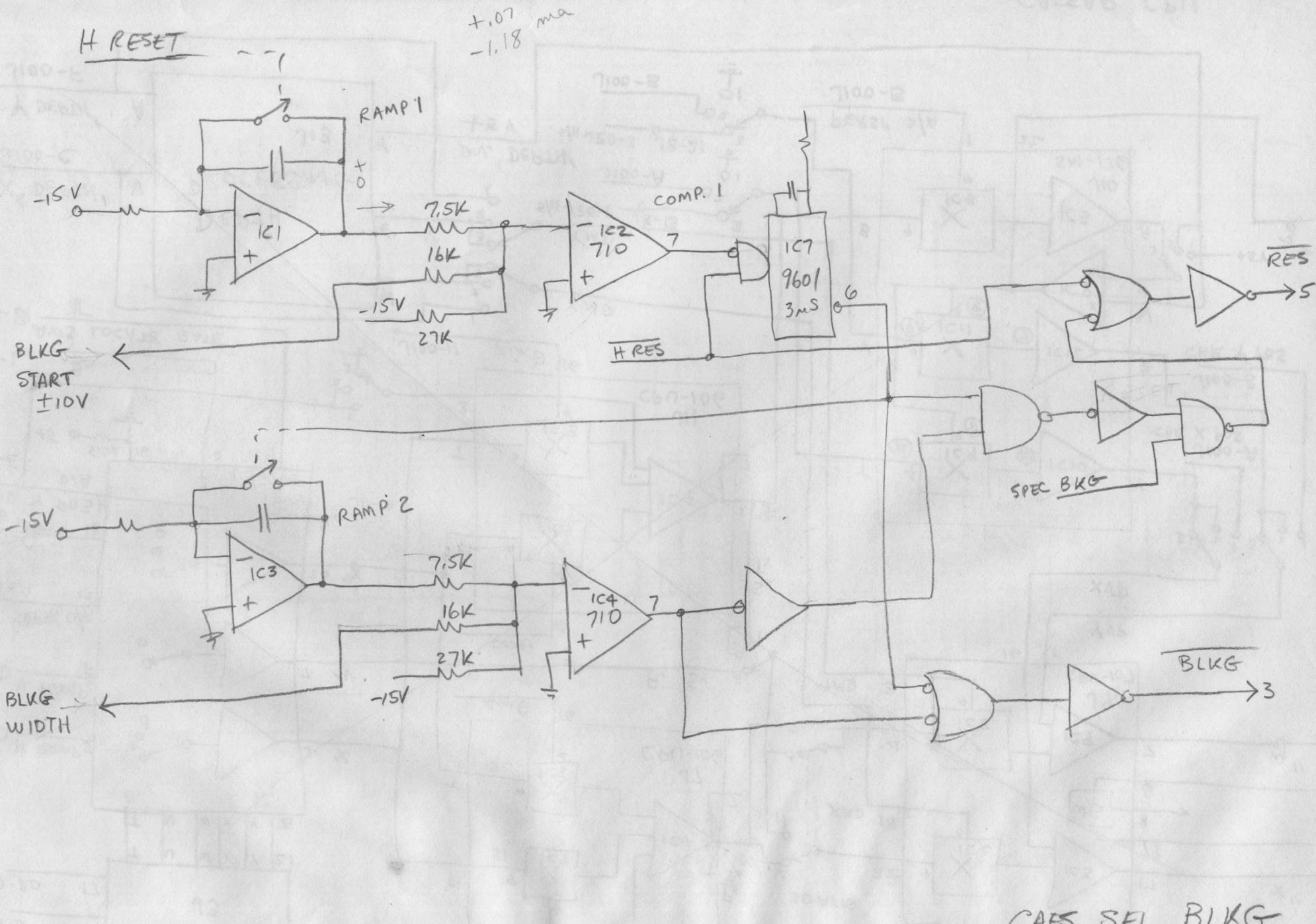


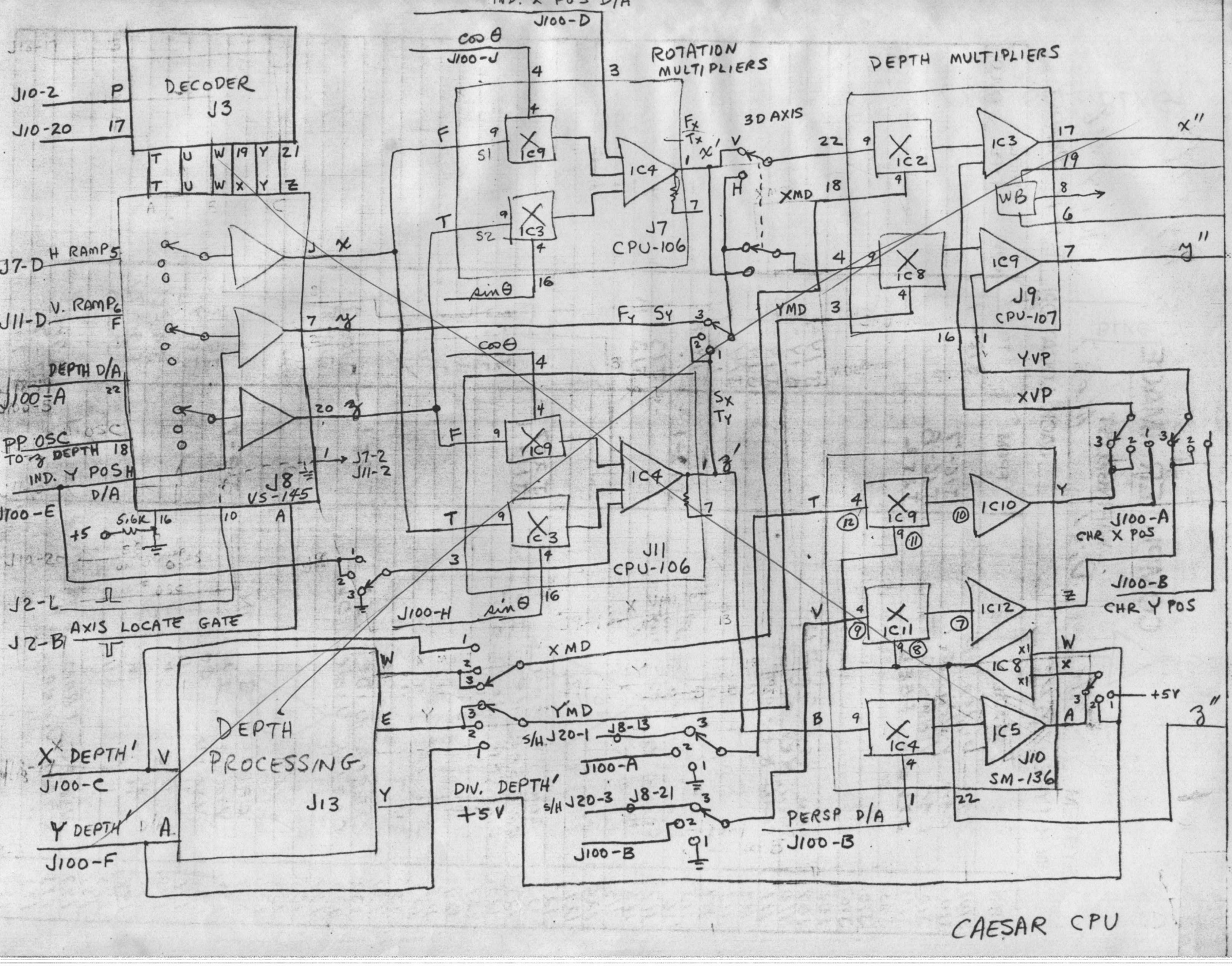

CAESAR CPU

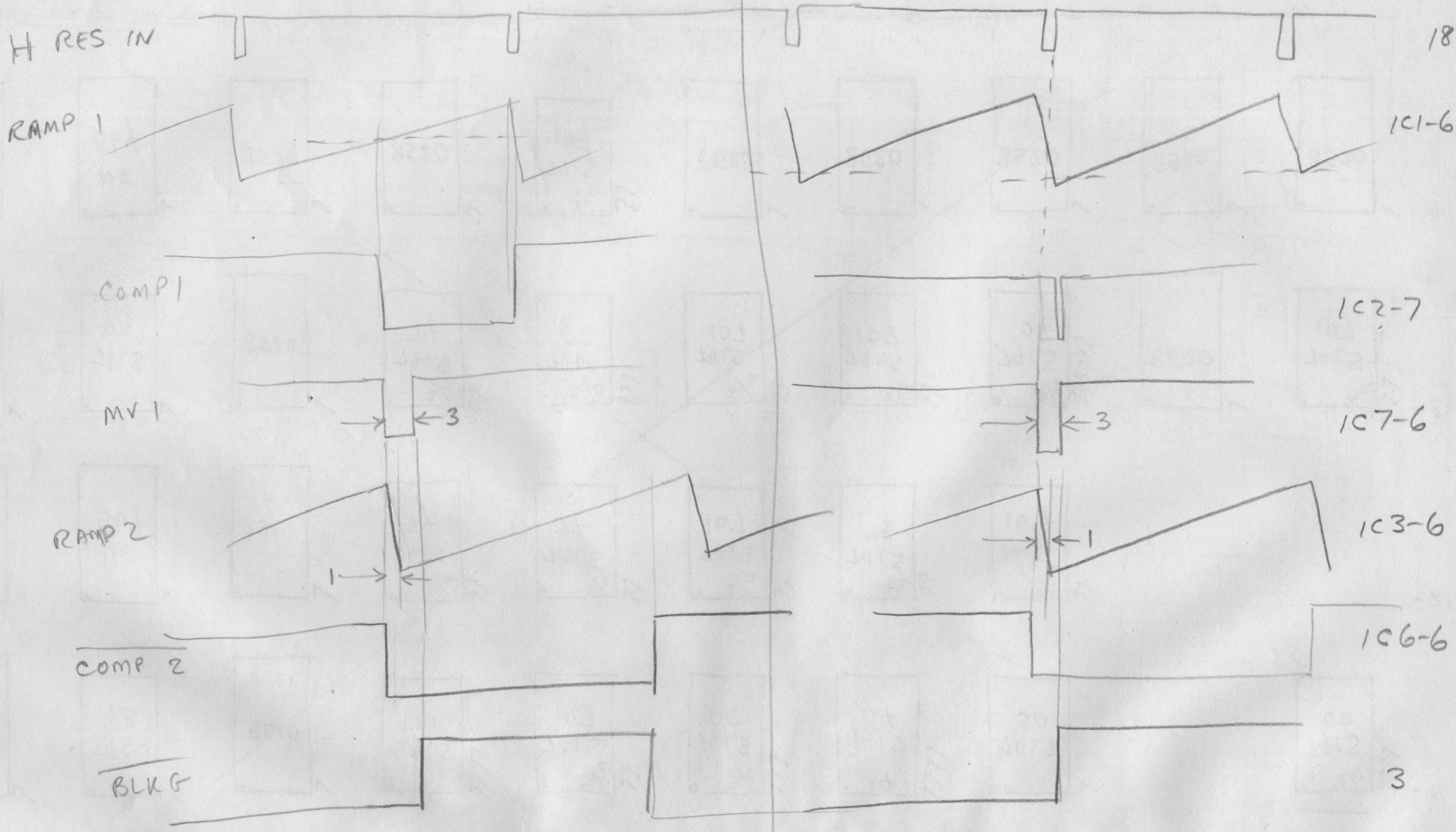
SYNC J4

BLANKING START
±10V
105K 1%
-15V
½ IH5020 IC8A
1000
+5 TV RATES
0 HI RES RATES
+15V
R5 15K
Q2 2N4351
R6 11K
95.3K 1%
-15V
5.1K
R4 24K
Q1 2N5134
HORIZ RESET
130K
-15
330K
+15V
R11 16K
R9 7.5K
R10 27K
15V
+5V
470
R17 20K
C9 470pf
C8 .01µf
IC7 9601 3µS
R16 1K
+5V
3µS
R15 5.1K
BLANKING WIDTH
±10V
105K 1%
-15V
½ IH5020 IC8B
1000
+15V
1µS
R19 15K
R20 1K
Q3 2N5134
R18 5.1K
300pF
30pf
+5V
11K
R22 95.3K 1%
Q4 2N4351
R23 7.5K
R24 27K
-15V
R25 16K
15V
26 90Ω
R29 5.1K
IC6 7400
IC5 7400
IC6 7400
IC5 7400
H. RES.
TO J7-5
IC5B 7400
IC6B 7400
IC6C 7400
IC8A 7400
SELECTIVE BLANKING
TO J2-4
FROM INTERFACE
+5V
1K
+ SHORT RAMP
0 NORM RAMP
SECTION BLANKING
R1 5.1Ω 1/2W
+15V
C1 80µf
GRD
TO PIN 7 OF ALL 7400's & 9601
R2 5.1Ω 1/2W
C2 80µf
-15V
R3 2.7Ω 1/2W
+5V
C3 80µf
TO PIN 14 OF ALL 7400's & 9601

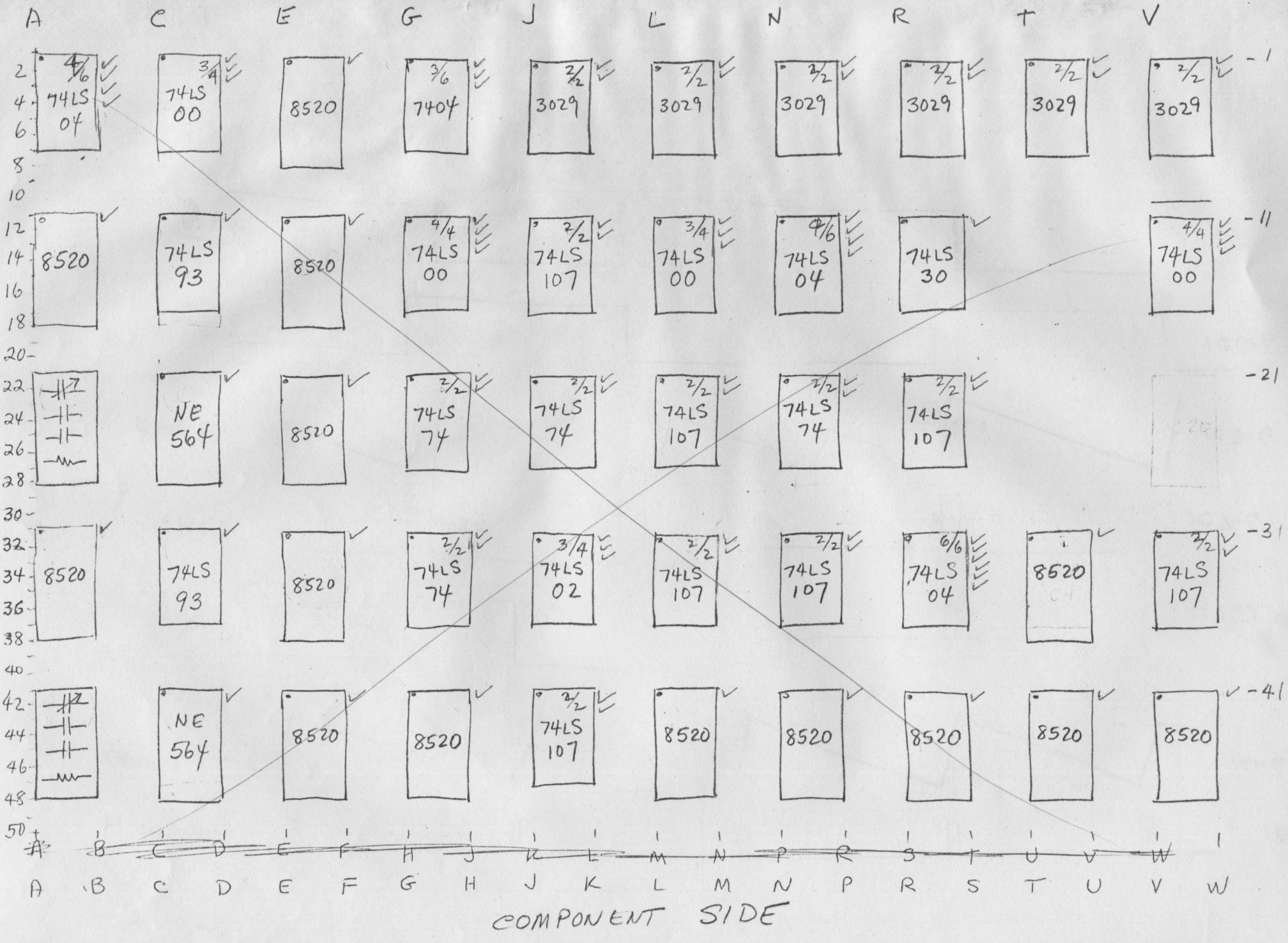
COMPUTER IMAGE
2475 W 2nd AVE
NONE
10-12-71
E R
CAESAR SELECTIVE BLANKING J18
C.P.U.
CPU-108


H RESET
+.07 ma
-1.18
RAMP 1
-15V
IC1
7.5K
16K
-15V
27K
BLKG START ±10V
IC2 710
COMP. 1
IC7 9601 3μS
H RES
RES
5
6
7
SPEC BKG
RAMP 2
-15V
IC3
7.5K
16K
27K
-15V
IC4 710
BLKG WIDTH
BLKG
3
CAES. SEL. BLKG

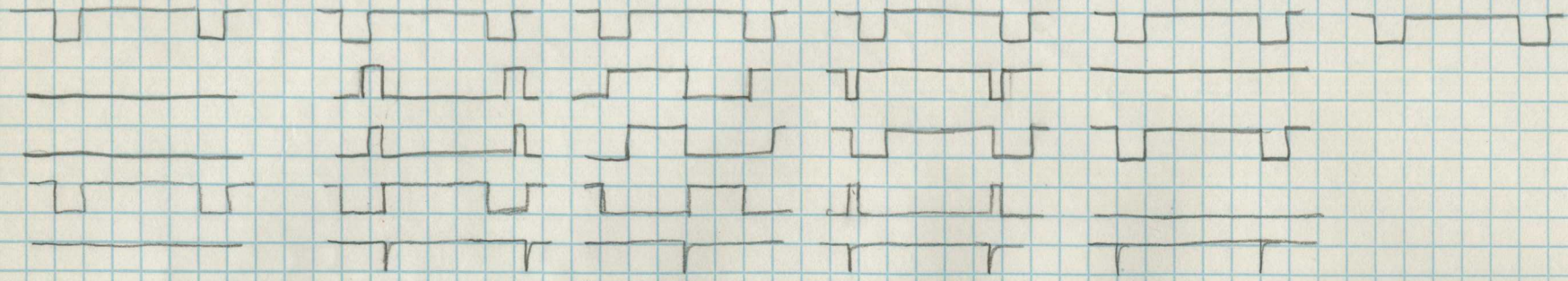

DECODER
J3
J10-2
J10-20
ROTATION MULTIPLIERS
DEPTH MULTIPLIERS
3D AXIS
J7
CPU-106
J9
CPU-107
J11
CPU-106
J8
VS-145
DEPTH PROCESSING
J13
J10
SM-136
H RAMP
V. RAMP
DEPTH D/A
J100-A
PP OSC
TO DEPTH
IND. Y POSH
D/A
AXIS LOCATE GATE
XMD
YMD
DIV. DEPTH'
PERSP D/A
J100-B
CHR X POS
CHR Y POS
YVP
XVP
+5V
CAESAR CPU

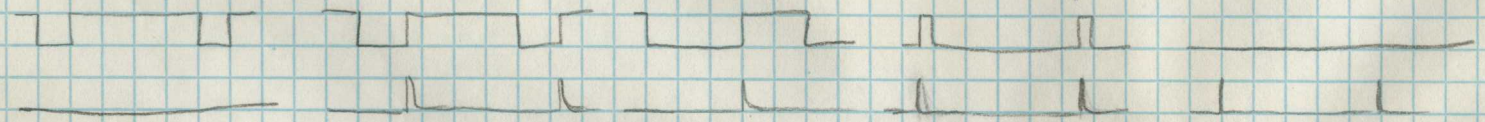

H RES IN
18
RAMP 1
IC1-6
COMP1
IC2-7
MV 1
3
3
IC7-6
RAMP 2
1
1
IC3-6
IC6-6
COMP 2
BLKG
3

5x.7 3.5
5x.9 4.5

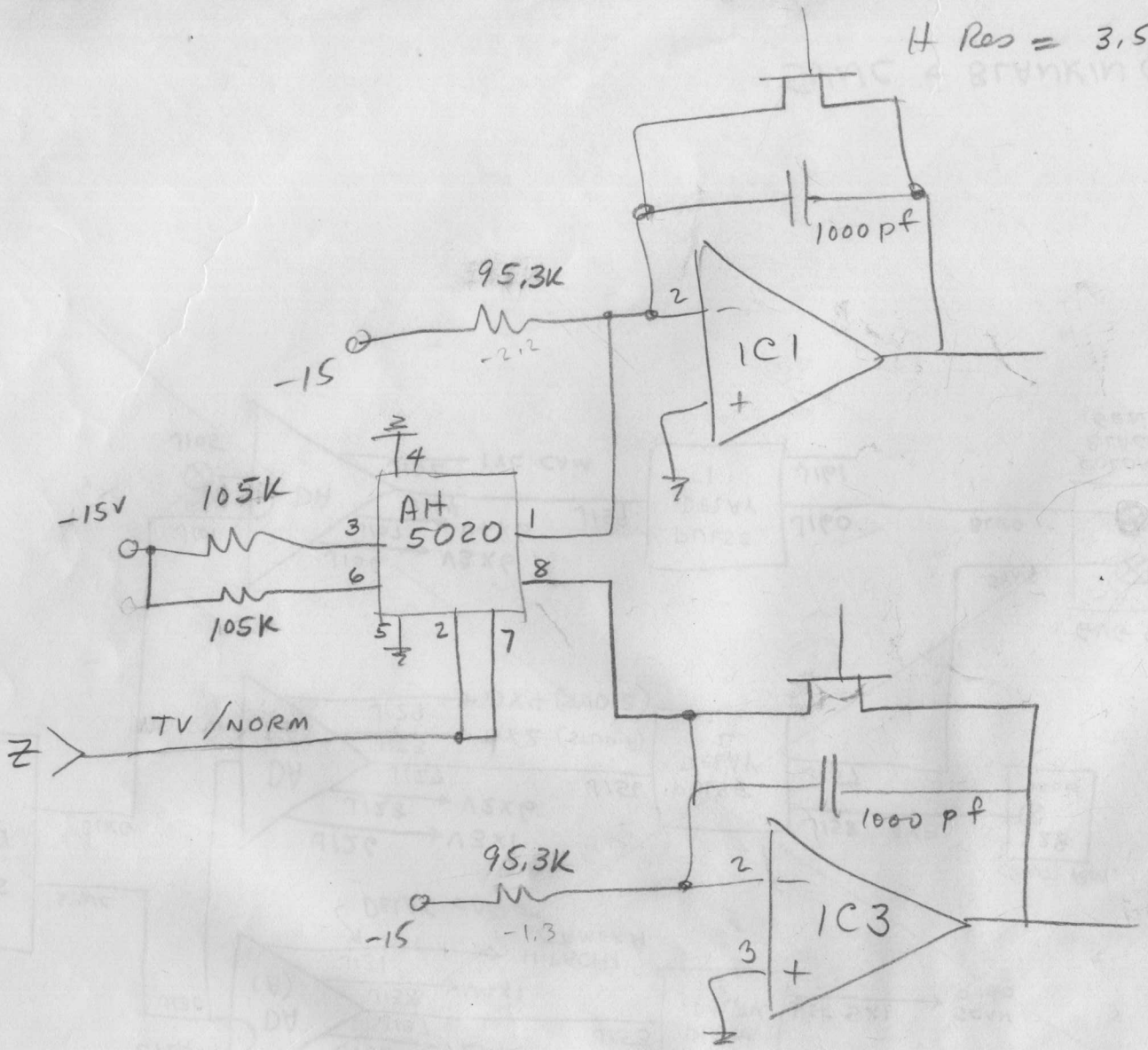



COMPONENT SIDE





H Res = 3.5 μS



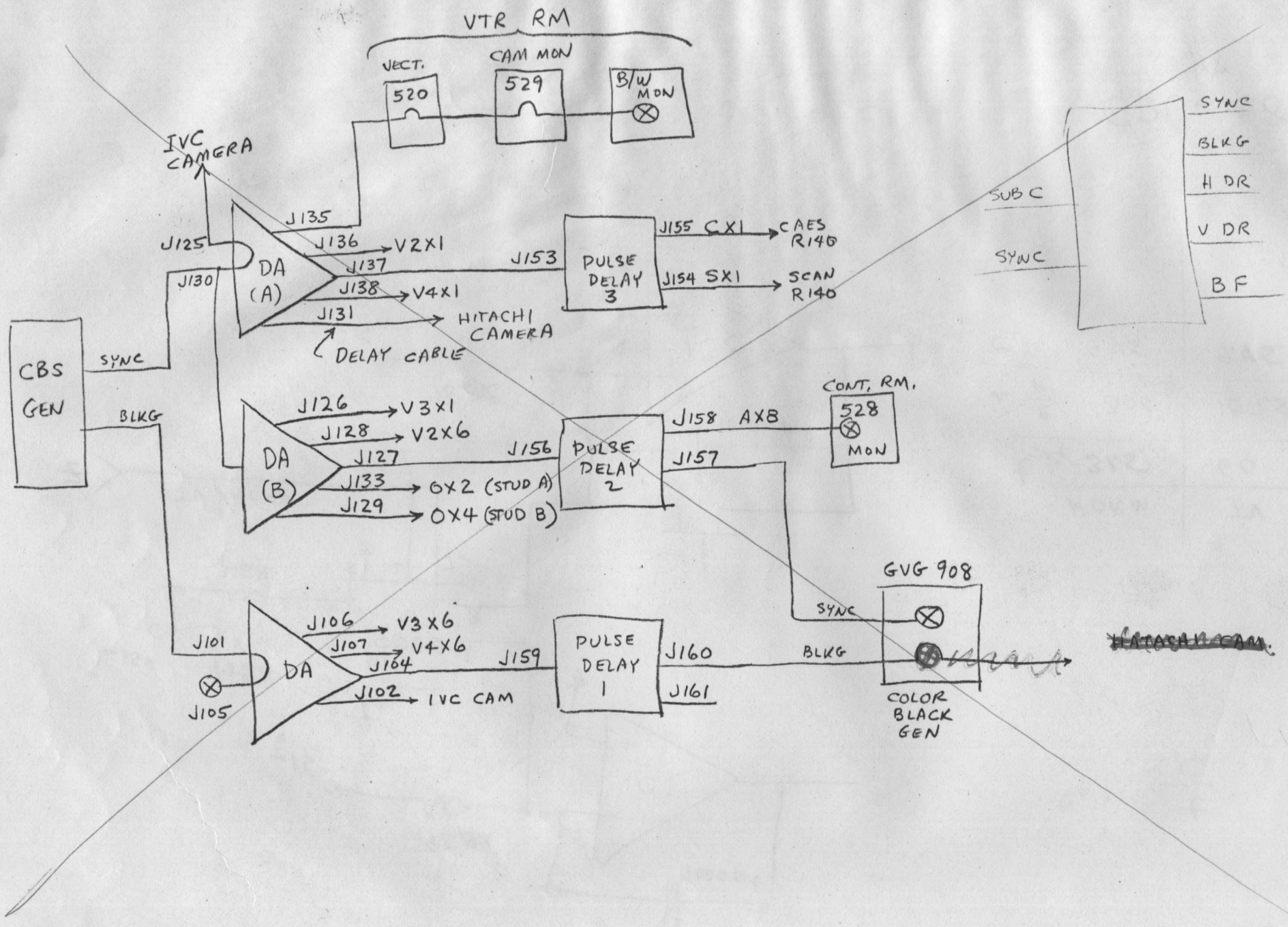

$$e_o = \frac{e_i\, t}{RC}$$

$$i = \frac{e_o\, C}{t}$$

167 μA

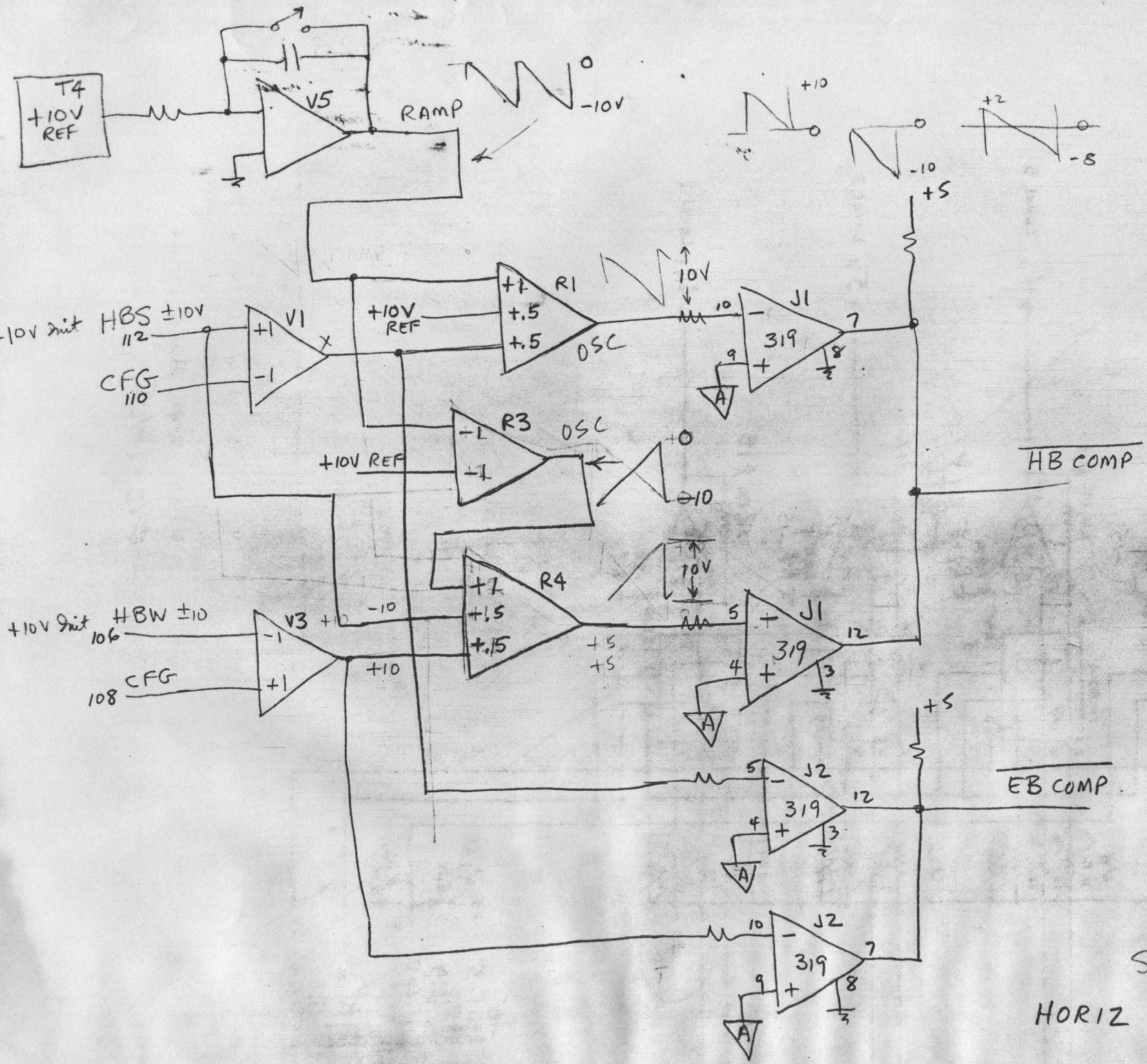
| | NORM | TV |
|---|---|---|
| $t_{\mu S}$ | 31.5 | 60 |
| $i = \frac{e}{R}$ | 300 μA | 157.5 |
| $e_o$ | 9.45 | 9.45 |

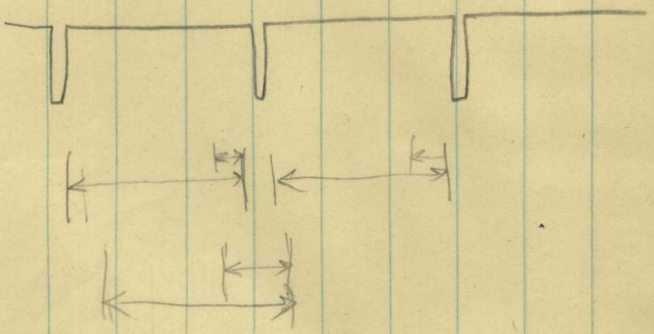
CPU-108
J18




SYNC + BLANKING

9-25-78


T4
+10V REF
V5
RAMP
0
-10V
+10
-10
+2
-8
+5
R1
+1
+.5
+.5
OSC
10V
10
J1
319
7
9
8
A
-10V Init
HBS ±10V
112
V1
+1
-1
X
CFG
110
+10V REF
R3
-1
-1
OSC
+10V REF
+0
-10
HB COMP
R4
+1
+1.5
+.15
10V
5
12
4
3
+5
+5
+10V Init
HBW ±10
106
V3
-1
+1
CFG
108
+10
-10
+10
J2
EB COMP
10
SYS 4
HORIZ BLANKING



H. RESET IN

RAMP 1 — START

COMP. 1

$\overline{\text{DMV 1}}$

RAMP 2 — WIDTH

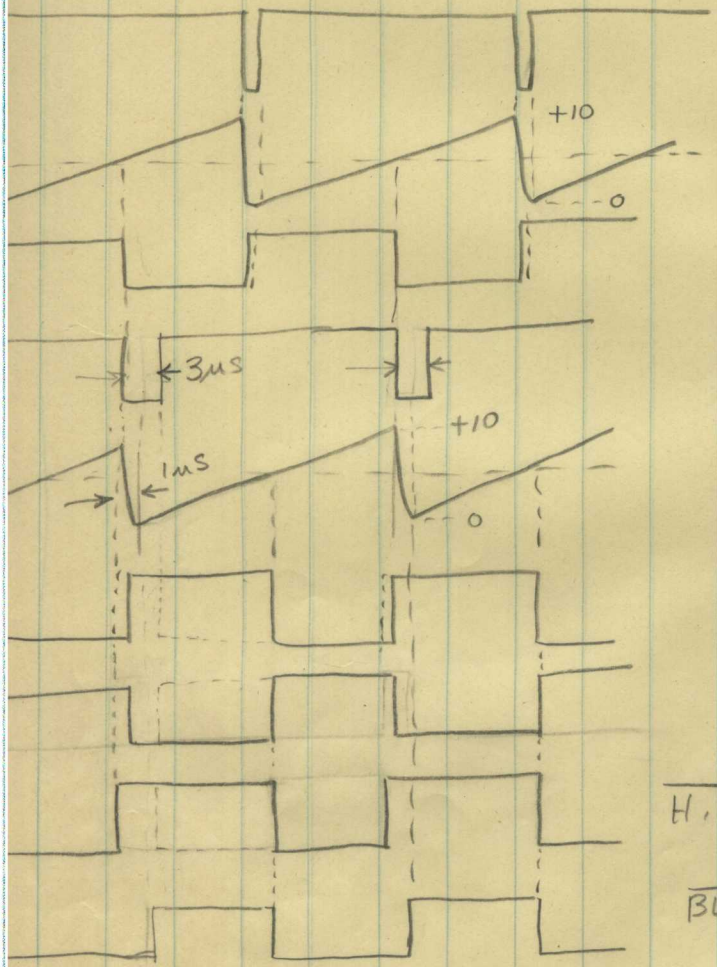
COMP. 2

$\overline{\text{COMP. 2}}$

DMV 1 + COMP. 2

$\overline{\text{DMV 1}} \times$ COMP. 2

| pin | Normal: | Blank: |
|---|---|---|
| 7 | Start +10V (+2047) | any |
| 19 | Width −10V (−2047) | +0V |




pin

18

IC1-6

IC2-7

IC7-6

IC3-6

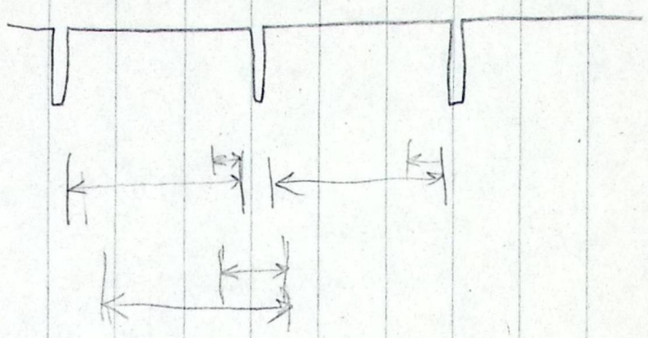
IC4-7

IC6-6

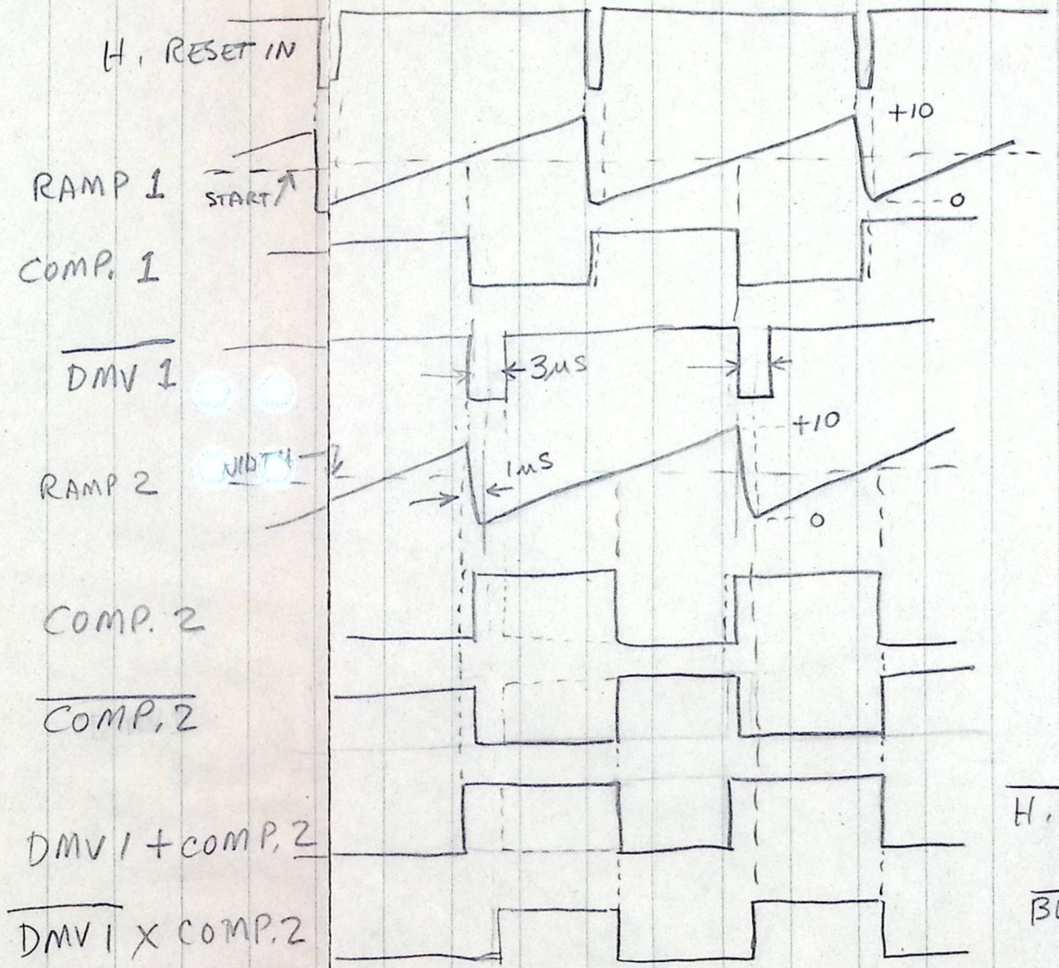
$\overline{\text{H. RESET}}$ OUT 5

$\overline{\text{BLKG}}$ OUT 3

CPU-108



| pin | Normal: | | Blank: |
|---|---|---|---|
| 7 | Start | +10V (+2047) | any |
| 19 | Width | -10V (-2047) | +0V |




| pin | |
|---|---|
| 18 | |
| | IC1-6 |
| | IC2-7 |
| | IC7-6 |
| | IC3-6 |
| | IC4-7 |
| | IC6-6 |
| 5 | H. RESET OUT |
| 3 | BLKG OUT |

CPU-108